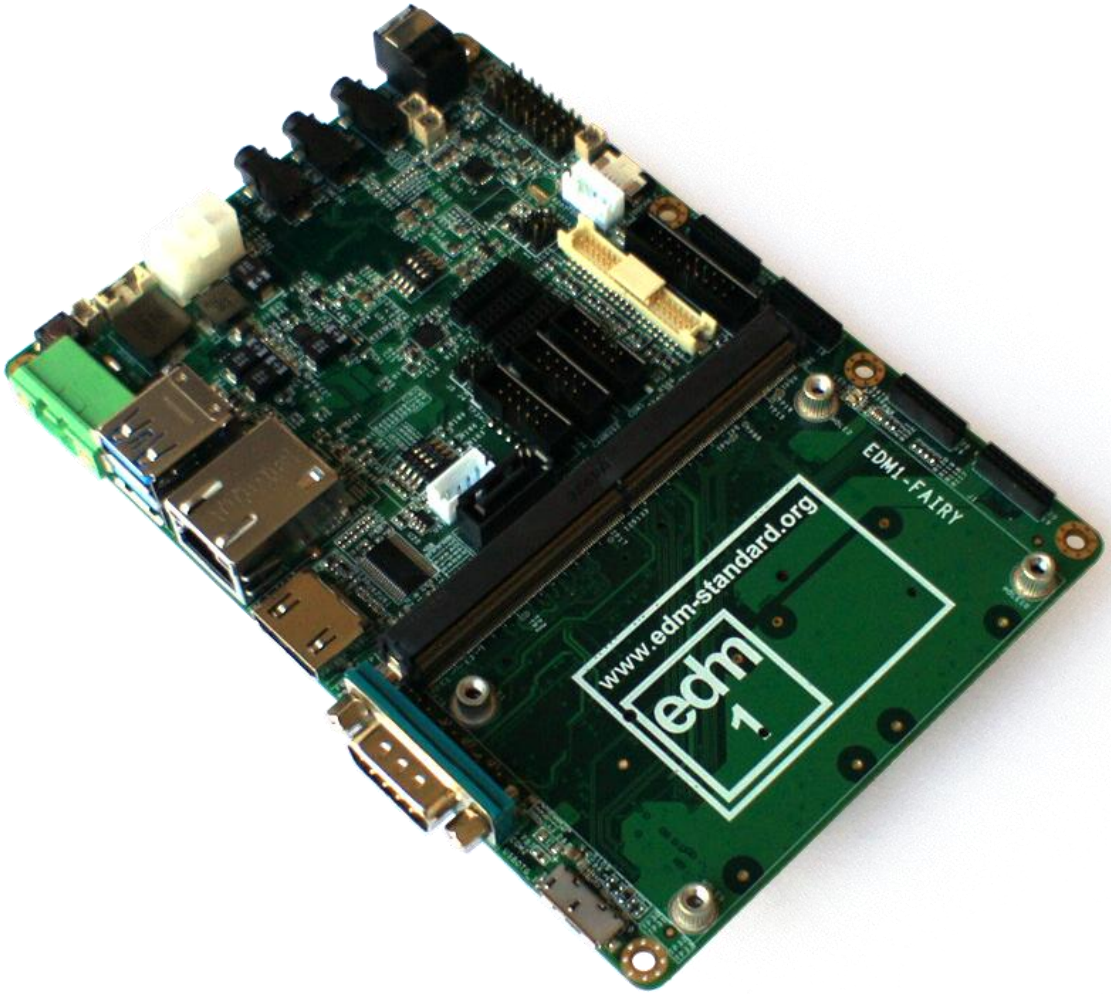



# EDM1

## CARRIER BOARD

# 1. Contents

# 3. Care and maintenance

## 3.1. General

Your device is a product of superior design and craftsmanship and should be treated with care. The following suggestions will help you.

- Keep the device dry. Precipitation, humidity, and all types of liquids or moisture can contain minerals that will corrode electronic circuits. If your device does get wet, allow it to dry completely.
- Do not use or store the device in dusty, dirty areas. Its moving parts and electronic components can be damaged.
- Do not store the device in hot areas. High temperatures can shorten the life of electronic devices, damage batteries, and warp or melt certain plastics.
- Do not store the device in cold areas. When the device returns to its normal temperature, moisture can form inside the device and damage electronic circuit boards.
- Do not attempt to open the device.
- Do not drop, knock, or shake the device. Rough handling can break internal circuit boards and fine mechanics.
- Do not use harsh chemicals, cleaning solvents, or strong detergents to clean the device.
- Do not paint the device. Paint can clog the moving parts and prevent proper operation.
- Unauthorized modifications or attachments could damage the device and may violate regulations governing radio devices.

These suggestions apply equally to your device, battery, charger, or any enhancement. If any device is not working properly, take it to the nearest authorized service facility for service.

## 3.2. Regulatory information

**Disposal of Waste Equipment by Users in Private Household in the European Union**

This symbol on the product or on its packaging indicates that this product must not be disposed of with your other household waste. Instead, it is your responsibility to dispose of your waste equipment by handing it over to a designated collection point for the recycling of waste electrical and electronic equipment. The separate collection and recycling of your waste equipment at the time of disposal will help to conserve natural resources and ensure that it is recycled in a manner that protects human health and the environment. For more information about where you can drop off your waste equipment for recycling, please contact your local city office, your household waste disposal service or the shop where you purchased the product.

CE

We hereby declare that the product is in compliance with the essential requirements and other relevant provisions of European Directive 1999/5/EC (radio equipment and telecommunications terminal equipment Directive).

**Federal Communications Commission (FCC) Unintentional emitter per FCC Part 15**

This device has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio or television reception. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause interference to radio and television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna
- Increase the separation between the equipment and receiver
- Connect the equipment to an outlet on a different circuit from that to which the receiver is connected
- Consult the dealer or an experienced radio/TV technician for help.

**WARNING!** To reduce the possibility of heat-related injuries or of overheating the computer, do not place the computer directly on your lap or obstruct the computer air vents. Use the computer only on a hard, flat surface. Do not allow another hard surface, such as an adjoining optional printer, or a soft surface, such as pillows or rugs or clothing, to block airflow. Also, do not allow the AC adapter to contact the skin or a soft surface, such as pillows or rugs or clothing, during operation. The computer and the AC adapter comply with the user-accessible surface temperature limits defined by the International Standard for Safety of Information Technology Equipment (IEC 60950).

# 4. Introduction

The EDM1 is a Carrier Board based on the EDM Type 1 standard.

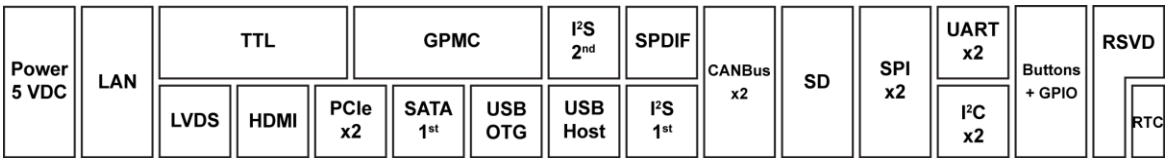



**Figure 1: supported interfaces on the EDM1 Carrier Board**

Support of certain interfaces depend on the System on Module that is used in combination with the EDM1 Carrier Board.

The EDM modules are typically being used as building blocks for portable and stationary embedded systems. The core CPU and support circuits, including DRAM, booth flash, power sequencing, CPU power supplies, Gigabit Ethernet and display interfaces are concentrated on the module. The modules are used with application specific carrier boards that implement other features such as audio CODECs, touch controllers, sensors and etcetera.

The modular approach offered by the EDM standard gives your project scalability, fast time to market and upgradability while reducing engineering risk and maintain a competitive total cost of ownership.

The SOM and its carrier board come in different versions, the user's guide is meant as a general guide for all these versions. Pictures and details of the device can differ from the actual purchased product. All specifications are subject to change without notice.

Visit our website for more details, to download this user guide or to see other information.

# 5. Getting started

## 5.1. Contents of the EDM1STAR


| | | | |
|---|---|---|---|
| 1 | EDM1 Carrier Board | 9 | 4 standoffs |
| 2 | 12V DC Power adapter | 10 | 4 bolts for the standoffs |
| 3 | Converter for the power adapter | 11 | DE9 cable for CAN BUS and COM1 (3x) |
| 4 | BS 1363 (Type G) power cord (UK) | 12 | SATA Data cable |
| 5 | CEE 7/4 (Type F) Power cord (EU) | 13 | SATA power cable |
| 6 | NEMA 5-15 (Type B) power cord (US) | 14 | EDM-MNF-BOOT PCB |
| 7 | USB 3.0 A to micro-USB B cable | 15 | RTC-battery |
| 8 | 4 screws to mount the System on Module | | |

**Table 1: contents of the EDM1START**

## 5.2. Additional products and accessories

**System on Module**

A EDM Type 1 System on Module is required to create fully functional development kit. The EDM1 carrier board is fully compatible with EDM Type1 System on modules.

**Display**

A HDMI monitor with a good HDMI cable can be used as a Display. Other Displays are also available, for example TDHJ070NA4RESKIT, which is a 7"LVDS Display with 4 wire resistive touch screen.

## 5.3. EDM-MNF-BOOT PCB

By default the board will boot first from iNAND / NAND Flash.

To force the board to boot from SD-card, the EDM-MNF-BOOT PCB should be inserted in the MNF Connector as shown in Figure 2 (white dot at orange arrow; jumpers facing inward). The boot order will change and it will first boot from SD-card.

The Jumper settings on the EDM-MNF-BOOT PCB depend on the System on Module, and can be found in the respective System on Module User guide.

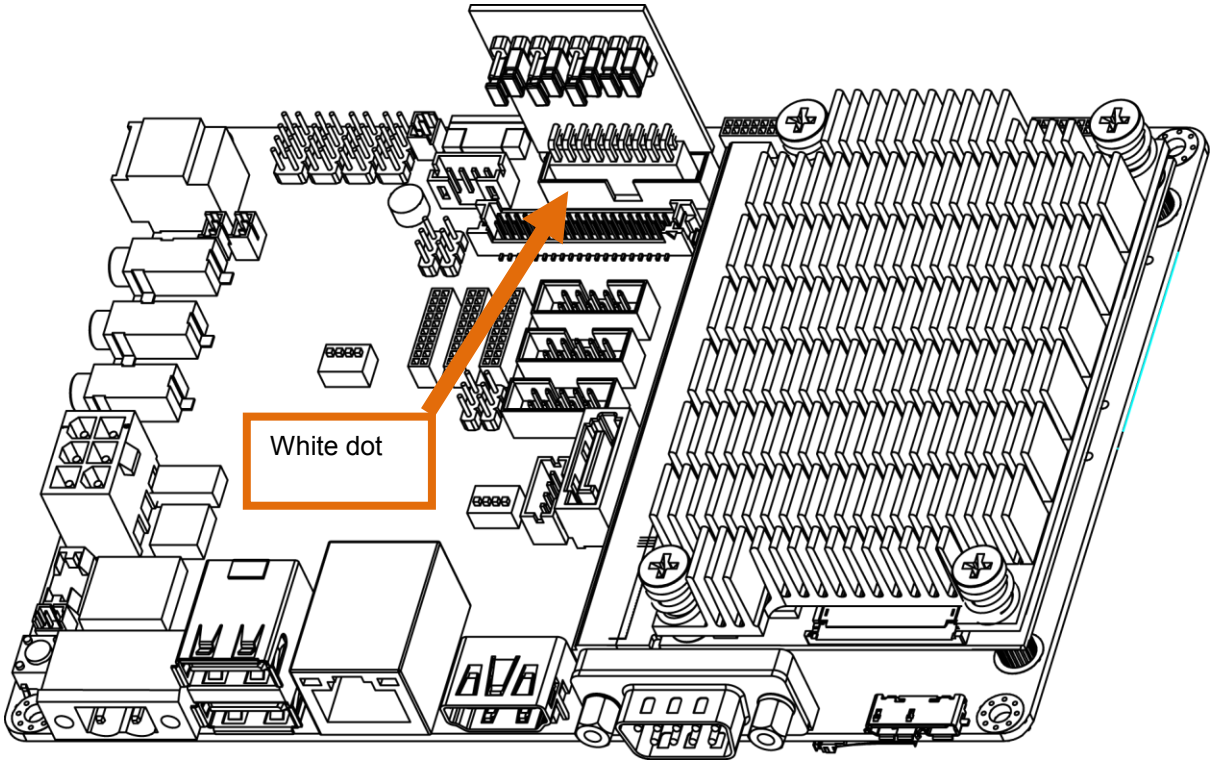



**Figure 2: the EDM-MNF-BOOT PCB inserted in the MNF connector**

## 5.4. Battery for RTC

The power for the RTC is supplied by a CR2032 battery which can be connected to the J8 connector on the carrier board.

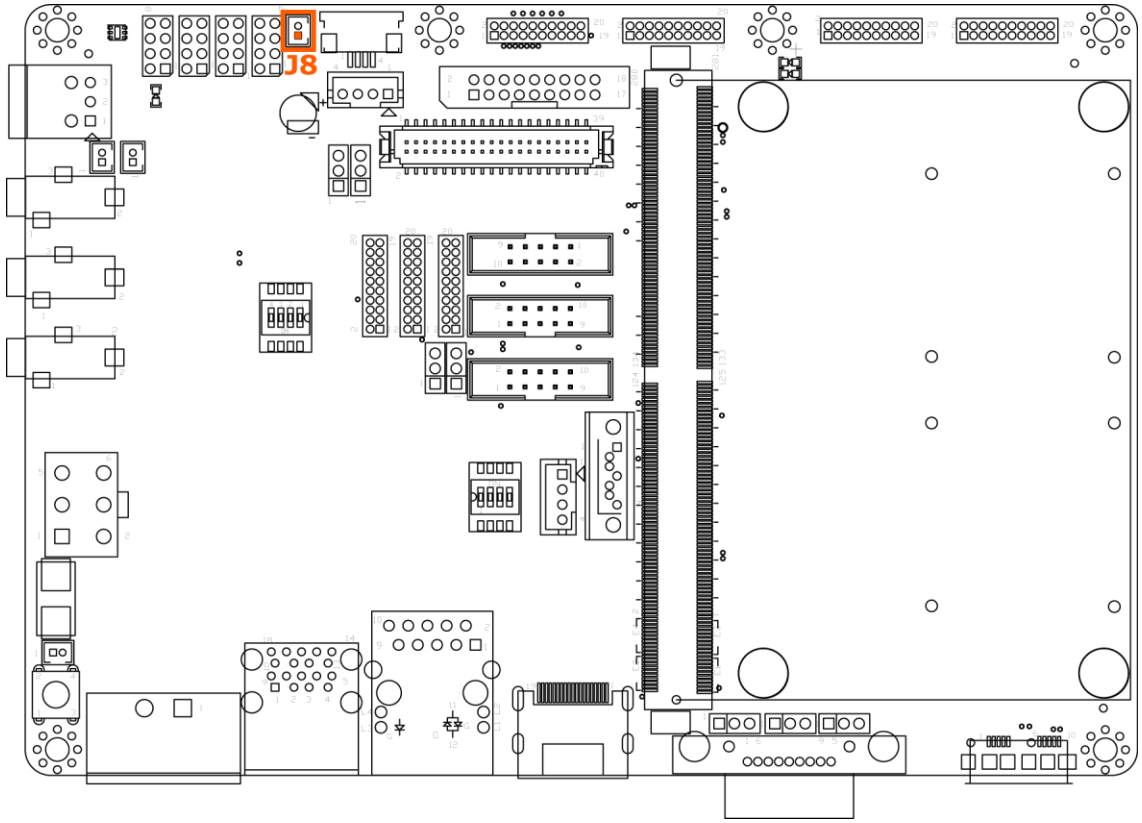



**Figure 3: Location of the RTC battery connector**

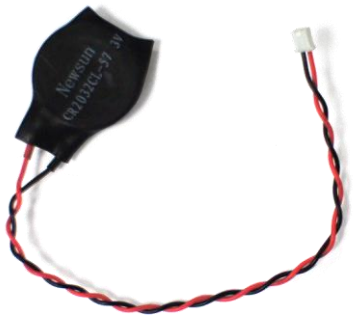


Figure 4: CR2032 Battery for RTC

## 5.5. Mounting an EDM Type 1 System on Module if Required

EDM System on modules are sold separately in Evaluation Start Kits. Ensure that your module is an EDM Type 1System on Module. Modules that require a heat sink will have them included inside the Evaluation Start Kit.  In case the evaluation start kit does not include a heat sink, steps 1 till 4 can be skipped.

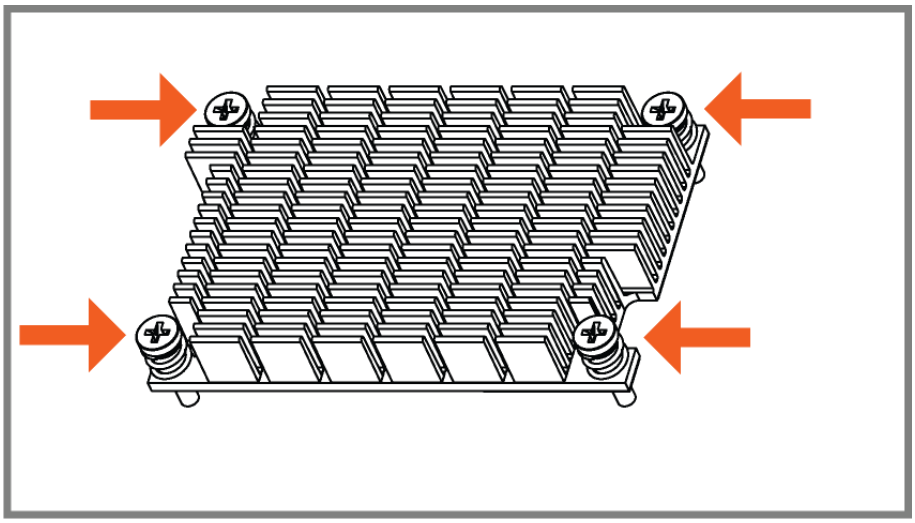


**Figure 5: Step 1 - Insert the screws**

Insert the screws (with springs), in the four corner holes of the heat sink.

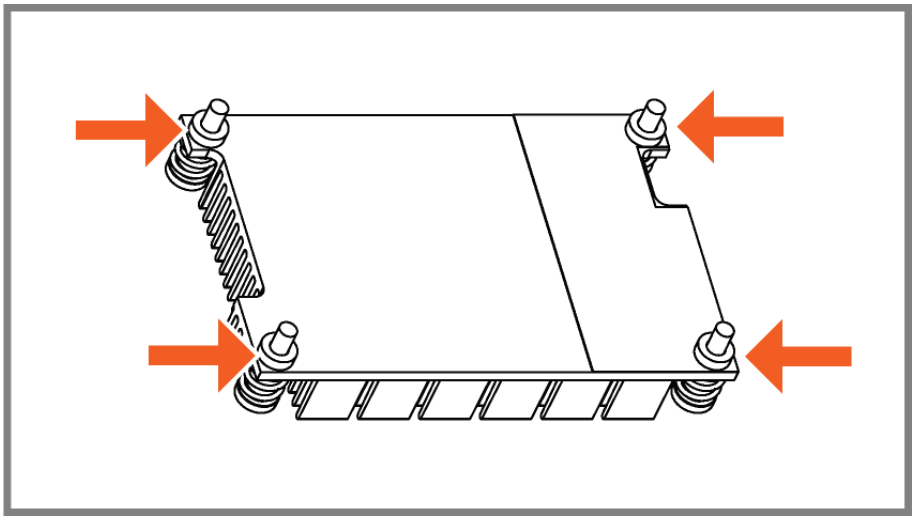


**Figure 6: Step 2 - Mount the washers**

Turn the assembly upside down. Mount the four washers on the screws.

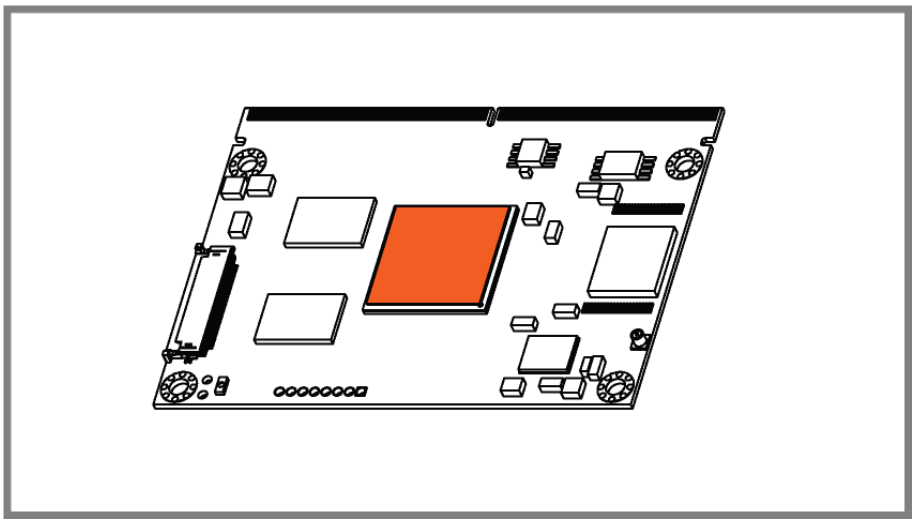


**Figure 7: Step3 - Place the thermopad (on the processor)**

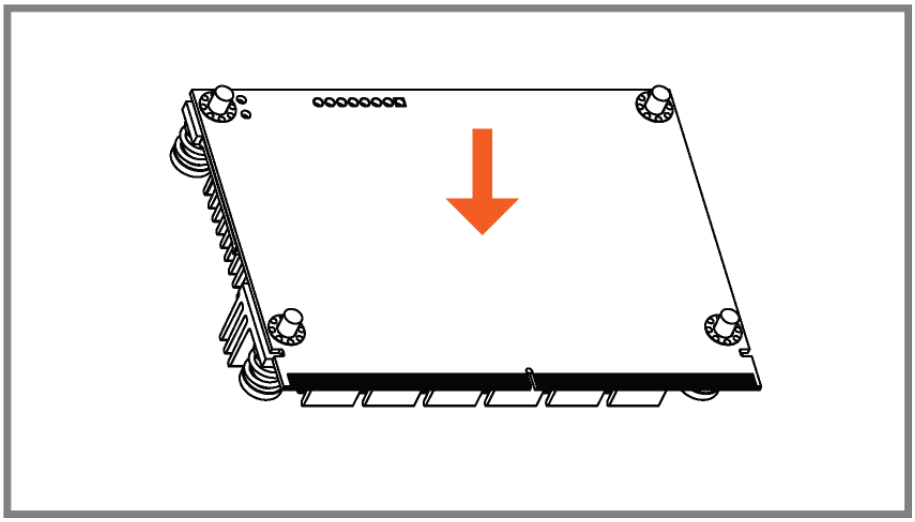


**Figure 8: Step4 - Place the module on the heat sink, and turn the assembly around.**

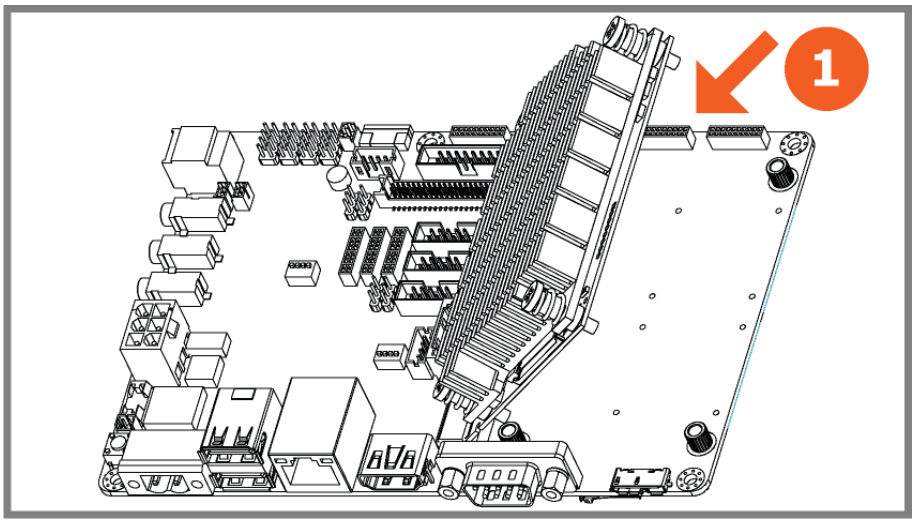



**Figure 9: Step5 - Insert the module in the carrier board**

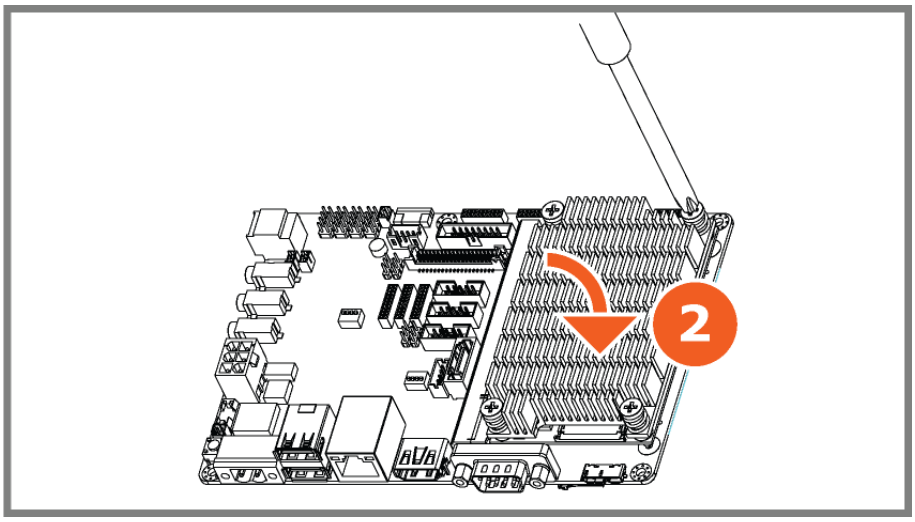



**Figure 10: Step6 - Press the module down and fasten the screws**

## 5.6. Mounting the standoffs

The standoffs should be mounted in the corners of the carrier board to place the board stable on a flat surface. This will also to allow airflow under the carrier board.

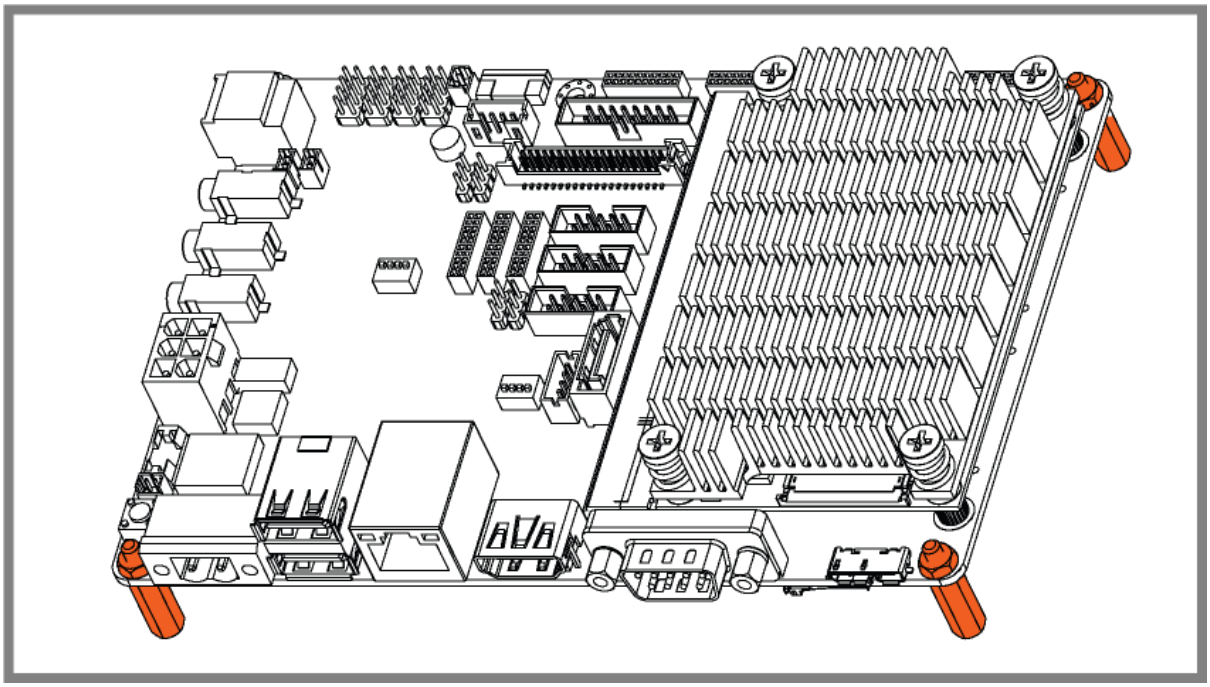


**Figure 11: standoffs and bolts mounted in the four corners of the carrier board**

## 5.7. Connecting a null modem cable to COM1

**Figure 12: The terminal cable connected with the DE9 cable to the COM1 (UART1) connector.**

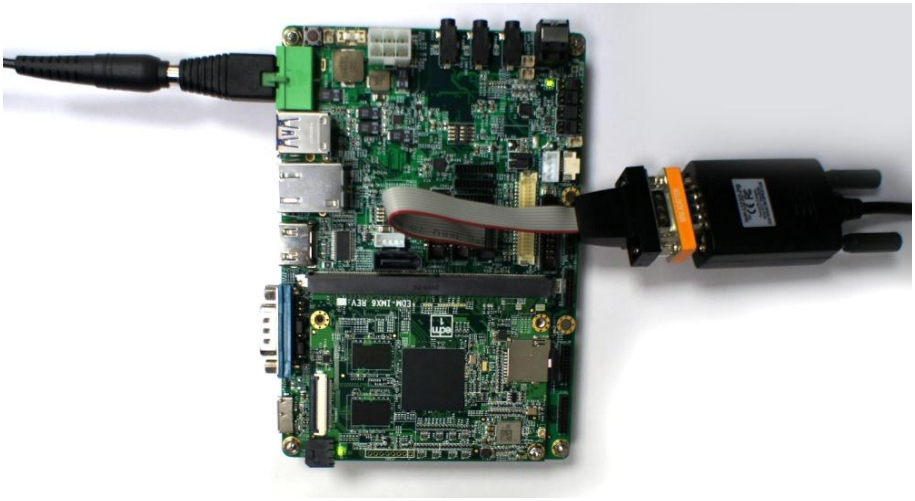


**Figure 13: The cable (RS-232 to USB) with null-modem-block connected with the DB9 cable to the COM1 (UART1) connector.**

Start PuTTY (a free telnet/ ssh client) on your computer and make sure the “Options controlling local serial lines” are as in Figure 14:

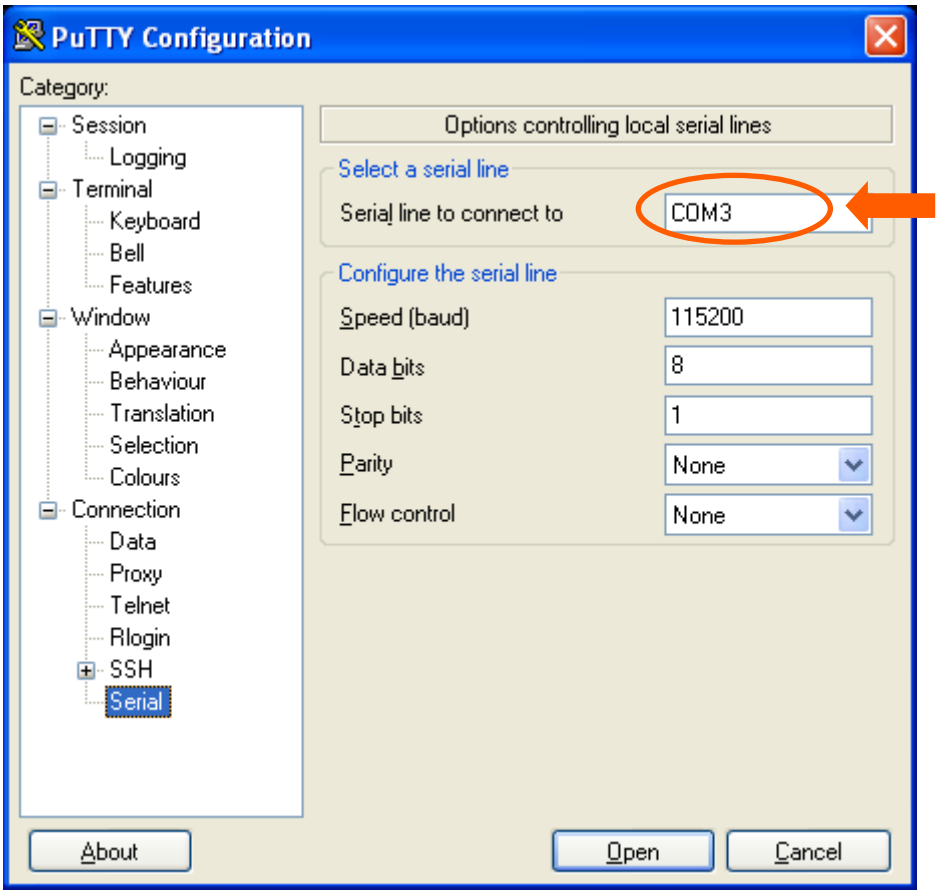



**Figure 14: Settings**

For computers running a Windows Operating System, more steps (see Figure 15 to Figure 18) might be required in order to check which serial line is used (see orange circle in Figure 14):


**Figure 15: Right click on "My Computer" and select Properties**

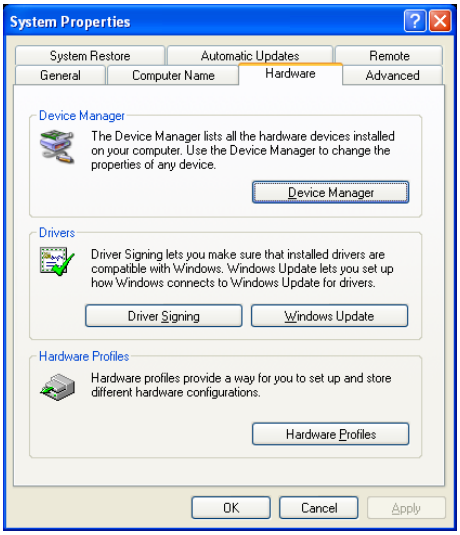



**Figure 16: Go to the hardware tab and select "Device manager"**

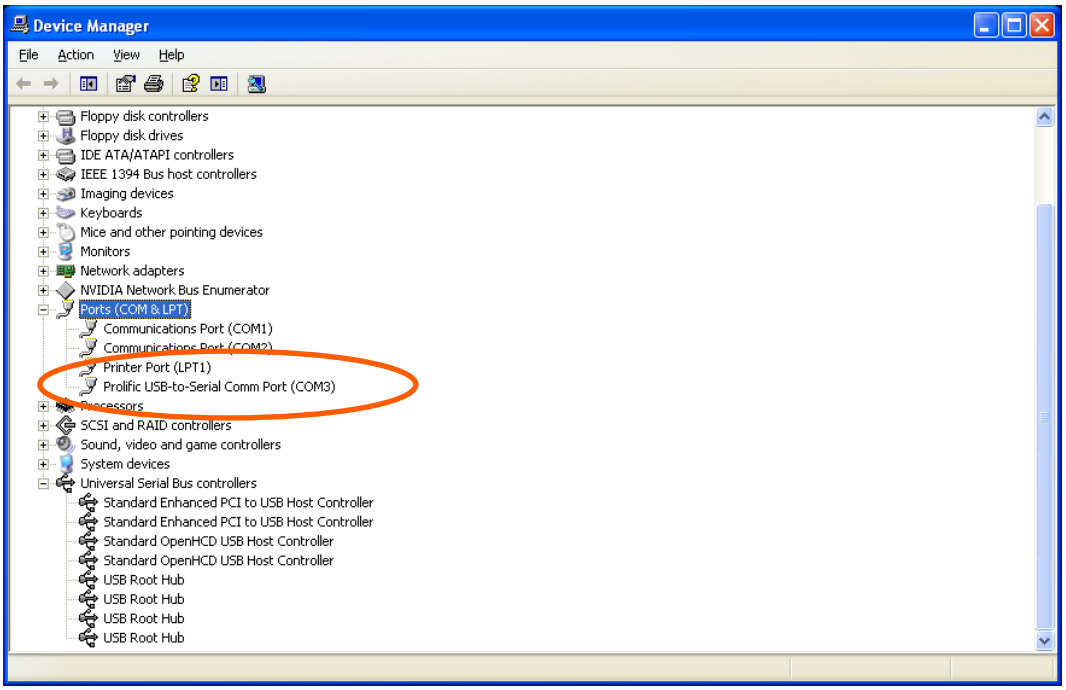



**Figure 17: Under Ports (COM & LPT) you will see the board connected with the null modem cable (in this picture COM3), this means in Putty the serial line should be changed into COM3.**

- Go to Session and check if “specify the destination you want to connect to “ is on Serial (See Figure 18)
- Press open and a window will pop up (see Figure 19)

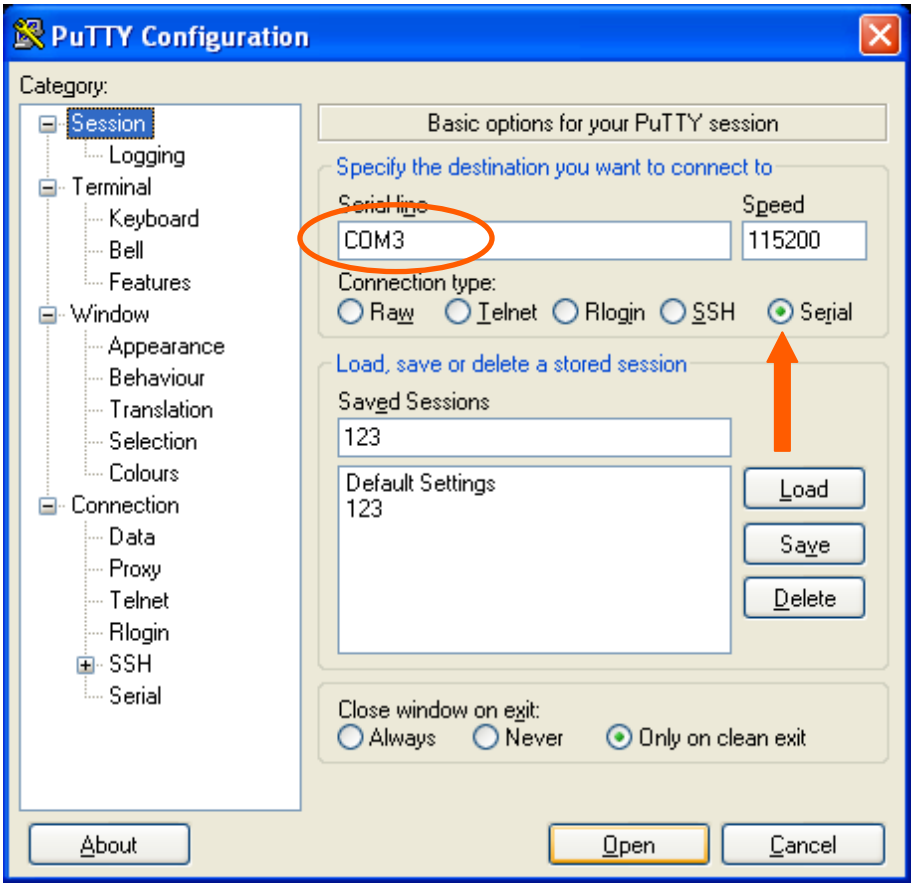



**Figure 18: check if serial is selected and then select open**

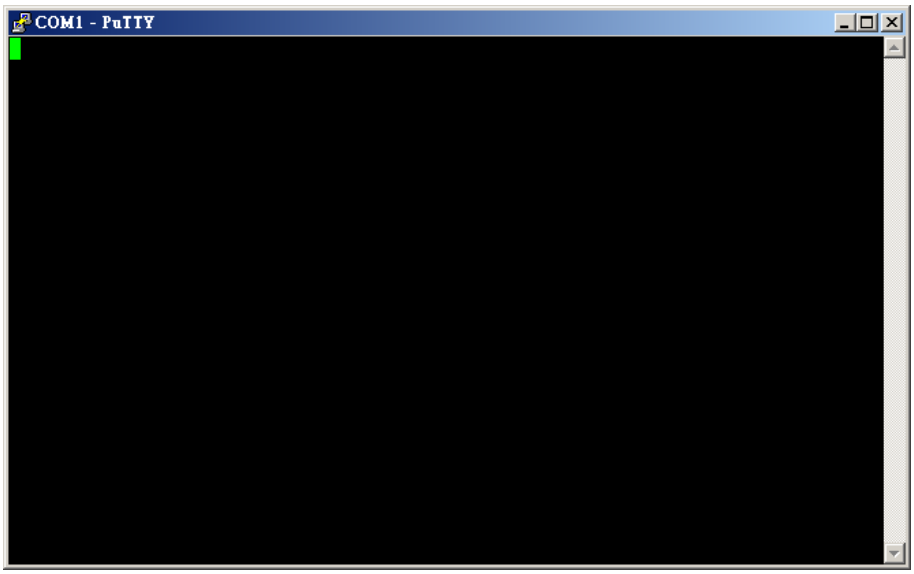



**Figure 19: PuTTY terminal window**

- You will now be able to see what is going on during the installation.
- If nothing happens then please check the settings and check if the cable is correctly connected to the UART1/COM1 pin header.

## 5.8. Block diagram

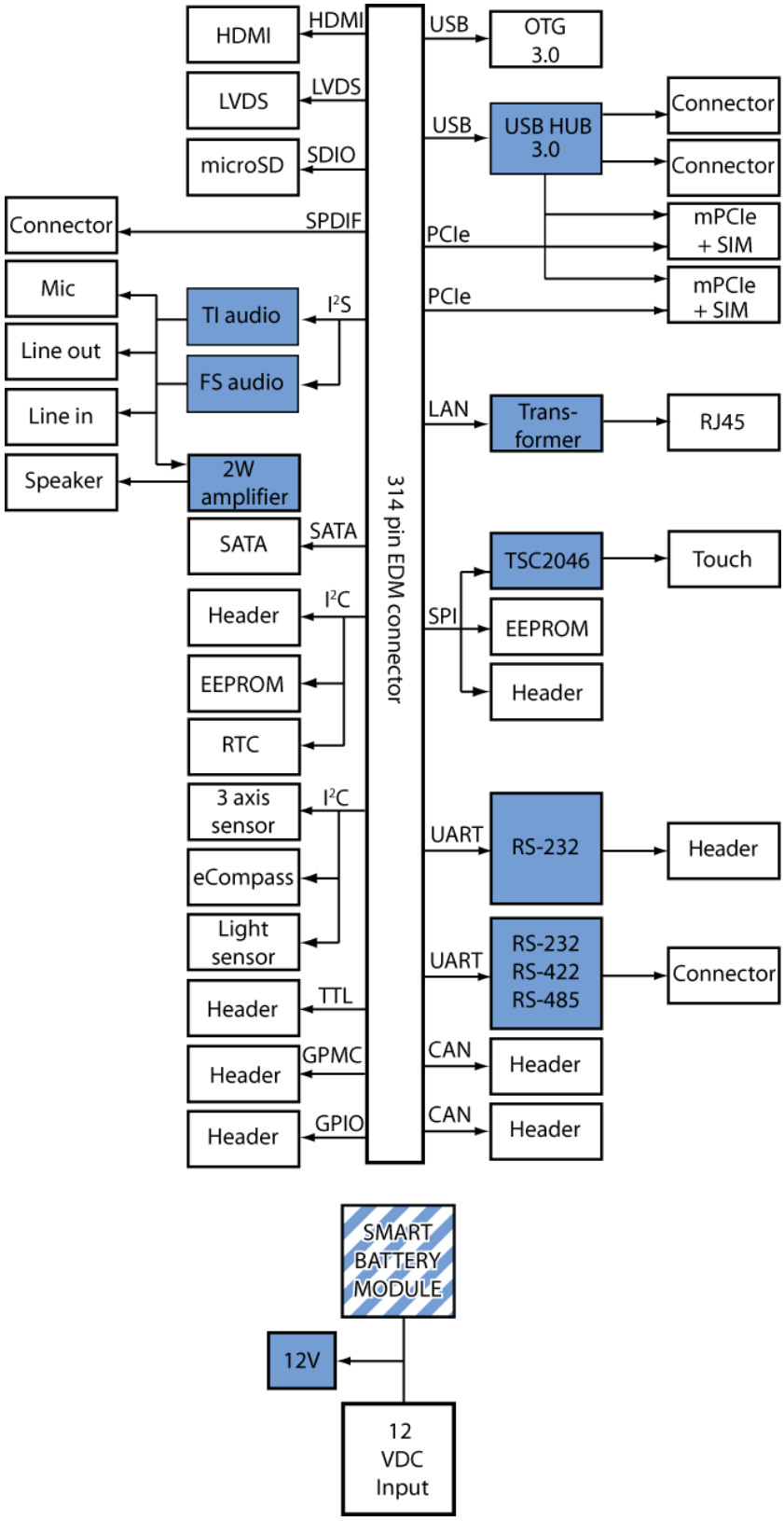



**Figure 20: Block diagram of the EDM1 Carrier Board**

## 5.9. EDM1 Carrier Board Overview

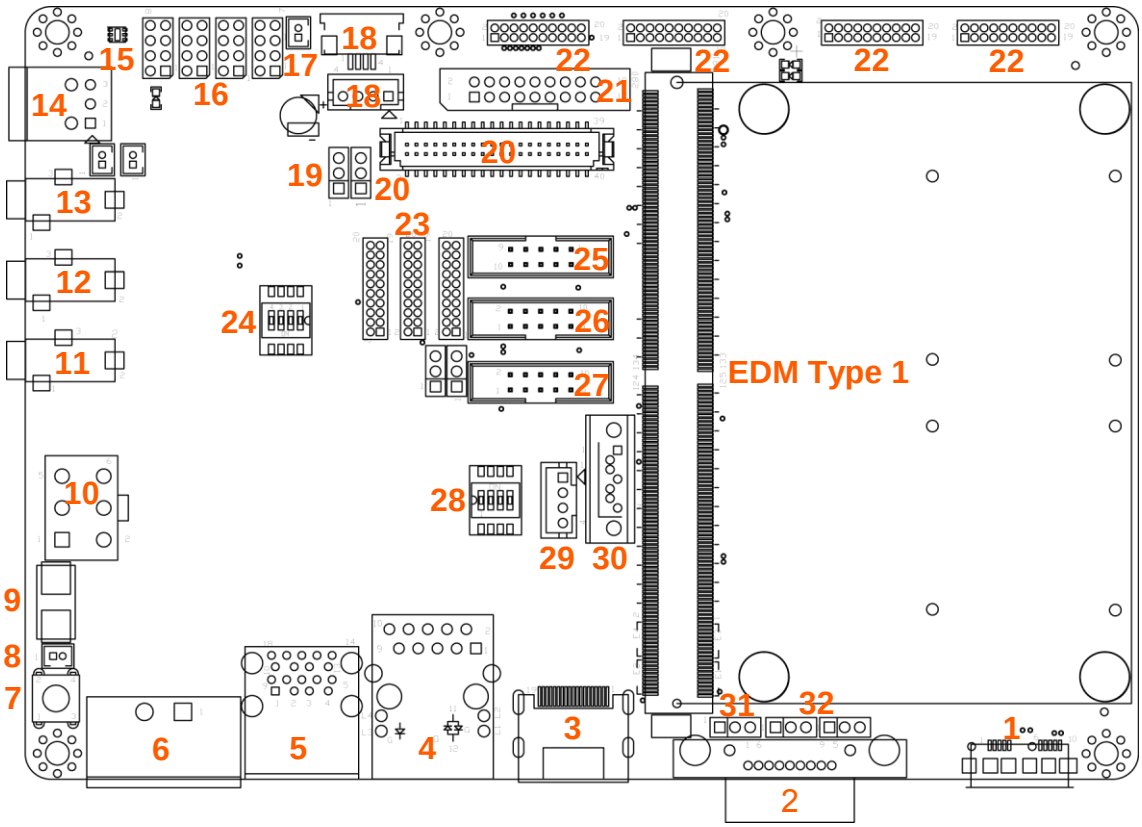



**Figure 21: EDM1 top view**

Top view

| # | function | # | function |
|---|---|---|---|
| 1 | USB-OTG 3.0 | 17 | RTC battery connector |
| 2 | COM 2: (RS232/422/485) | 18 | 4 wire touch connectors |
| 3 | HDMI connector | 19 | 4 wire touch ON/OFF jumper |
| 4 | RJ45 Gigabit LAN connector | 20 | LVDS connector and 6/8 bit selection jumper |
| 5 | USB Host (2x) | 21 | MNF connector |
| 6 | Power connector 12V DC (Phoenix Combicon MSTB 2.5) | 22 | Expansion connectors |
| 7 | Reset switch | 23 | GPMC connectors |
| 8 | power switch connector | 24 | audio select switch SW2 |
| 9 | Fuse | 25 | COM1 connector |
| 10 | Smart battery connector | 26 | CAN BUS2 connector |
| 11 | Microphone | 27 | CAN BUS1 connector |
| 12 | Line in | 28 | COM2/ audio selection switch |
| 13 | Line out | 29 | SATA power connector |
| 14 | S/P Dif | 30 | SATA data connector |
| 15 | light sensor | 31 | USB-OTG jumper to select client/host |
| 16 | I2C selection jumper | 32 | WAN ON/ OFF Jumpers for mPCIe slots |

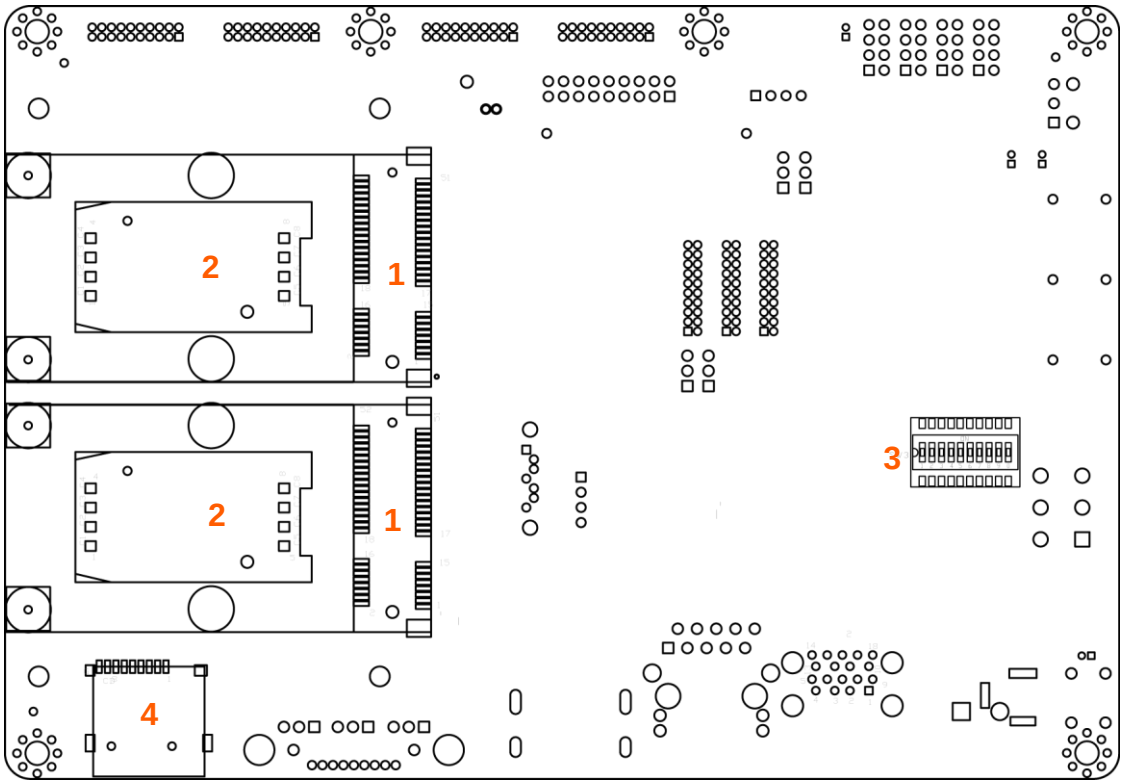


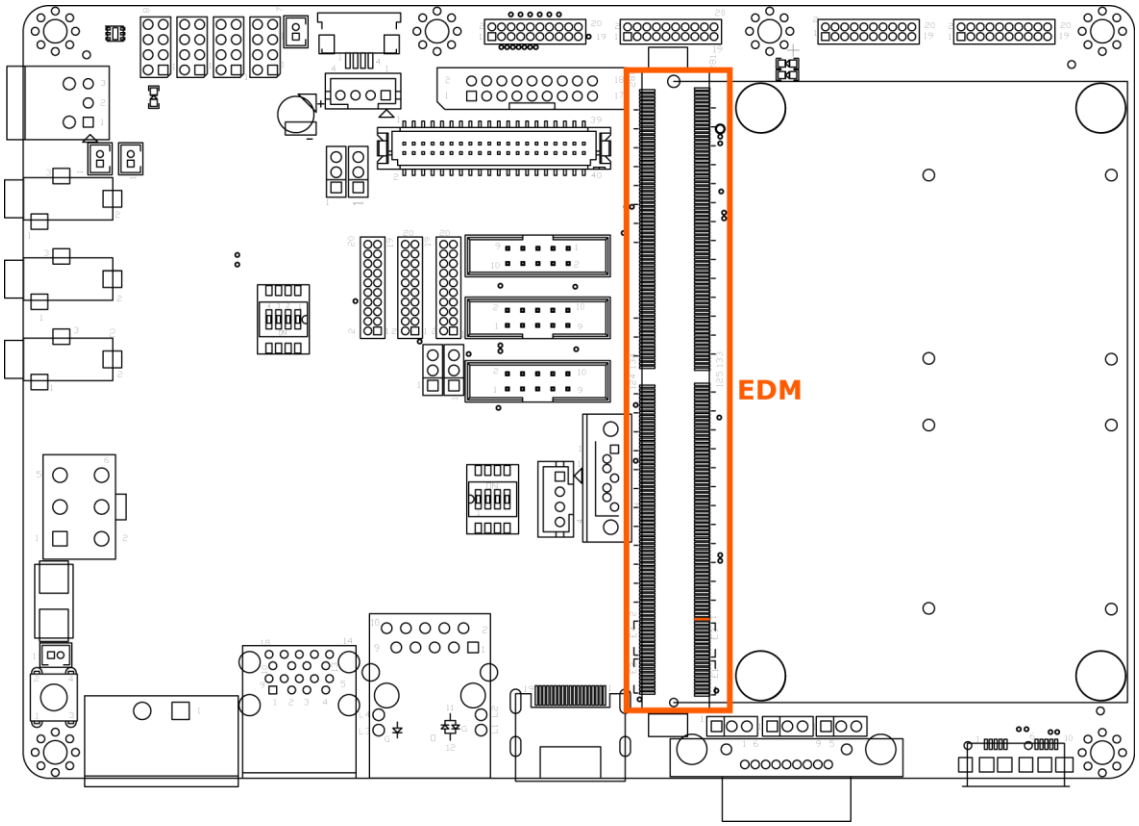

**Figure 22: EDM1 bottom view**

Bottom view

| # | function | # | function |
|---|---|---|---|
| 1 | Mini PCIe connector | 3 | Audio select switch |
| 2 | SIM card slot | 4 | micro SD-card slot |

# 6. Connector - Pin outs

## 6.1. EDM Type 1 Connector




The EDM connector 314 pin assignment for type 1 are listed in the table below.

| Pin # | EDM | Signal | V | I/O | Description |
|---|---|---|---|---|---|
| E1_1 | NC | 5VSB | 5VSB | P | Standby Power Supply 5VDC ± 5% |
| E2_1 | NC | 5VSB | 5VSB | P | Standby Power Supply 5VDC ± 5% |
| E1_2 | | VCC | 5V | P | Power Supply 5VDC ± 5% |
| E2_2 | | VCC | 5V | P | Power Supply 5VDC ± 5% |
| E1_3 | | VCC | 5V | P | Power Supply 5VDC ± 5% |
| E2_3 | | VCC | 5V | P | Power Supply 5VDC ± 5% |
| E1_4 | | VCC | 5V | P | Power Supply 5VDC ± 5% |
| E2_4 | | VCC | 5V | P | Power Supply 5VDC ± 5% |
| E1_5 | | VCC | 5V | P | Power Supply 5VDC ± 5% |
| E2_5 | | VCC | 5V | P | Power Supply 5VDC ± 5% |
| E1_6 | | VCC | 5V | P | Power Supply 5VDC ± 5% |
| E2_6 | | VCC | 5V | P | Power Supply 5VDC ± 5% |
| E1_7 | | VCC | 5V | P | Power Supply 5VDC ± 5% |
| E2_7 | | VCC | 5V | P | Power Supply 5VDC ± 5% |
| E1_8 | | VCC | 5V | P | Power Supply 5VDC ± 5% |
| E2_8 | | VCC | 5V | P | Power Supply 5VDC ± 5% |
| E1_9 | | VCC | 5V | P | Power Supply 5VDC ± 5% |
| E2_9 | | VCC | 5V | P | Power Supply 5VDC ± 5% |
| E1_10 | | VCC | 5V | P | Power Supply 5VDC ± 5% |
| E2_10 | | VCC | 5V | P | Power Supply 5VDC ± 5% |
| E3_1 | | GND | GND | P | Ground |
| E4_1 | | GND | GND | P | Ground |
| E3_2 | | GBE_MDI2+ | LAN | I/O | Gigabit Ethernet Media Dependent Interface (MDI) differential pair 2 positive signal |

| Pin # | EDM | Signal | V | I/O | Description |
|---|---|---|---|---|---|
| E4_2 | | GBE_MDI0+ | LAN | I/O | Gigabit Ethernet Media Dependent Interface (MDI) differential pair 0 positive signal |
| E3_3 | | GBE_MDI2- | LAN | I/O | Gigabit Ethernet Media Dependent Interface (MDI) differential pair 2 negative signal |
| E4_3 | | GBE_MDI0- | LAN | I/O | Gigabit Ethernet Media Dependent Interface (MDI) differential pair 0 negative signal |
| E3_4 | | GND | GND | P | Ground |
| E4_4 | | GND | GND | P | Ground |
| E3_5 | | GBE_MDI3+ | LAN | I/O | Gigabit Ethernet Media Dependent Interface (MDI) differential pair 3 positive signal |
| E4_5 | | GBE_MDI1+ | LAN | I/O | Gigabit Ethernet Media Dependent Interface (MDI) differential pair 1 positive signal |
| E3_6 | | GBE_MDI3- | LAN | I/O | Gigabit Ethernet Media Dependent Interface (MDI) differential pair 3 negative signal |
| E4_6 | | GBE_MDI1- | LAN | I/O | Gigabit Ethernet Media Dependent Interface (MDI) differential pair 1 negative signal |
| E3_7 | | LED1_ACT | CMOS 3.3V | O | Gigabit Ethernet LED Activity indicator |
| E4_7 | | GND | GND | P | Ground |
| E3_8 | | GND | GND | P | Ground |
| E4_8 | | LED1_nLink100 | CMOS 3.3V | O | Gigabit Ethernet 100Mbit/sec LED link indicator |
| E3_9 | | LVDS_A0- | LVDS | O | LVDS primary channel differential pair 0 negative signal |
| E4_9 | | LED1_nLink1000 | CMOS 3.3V | O | Gigabit Ethernet 1000Mbit/sec LED link indicator |
| E3_10 | | LVDS_A0+ | LVDS | O | LVDS primary channel differential pair 0 positive signal |
| E4_10 | | GND | GND | P | Ground |
| 1 | | GND | GND | P | Ground |
| 2 | | LCD_D0 | TTL | O | LCD Pixel Data bit 0 |
| 3 | | LVDS_A1- | LVDS | O | LVDS primary channel differential pair 1 negative signal |
| 4 | | LCD_D1 | TTL | O | LCD Pixel Data bit 1 |
| 5 | | LVDS_A1+ | LVDS | O | LVDS primary channel differential pair 1 positive signal |
| 6 | | GND | GND | P | Ground |
| 7 | | GND | GND | P | Ground |
| 8 | | LCD_D2 | TTL | O | LCD Pixel Data bit 2 |
| 9 | | LVDS_A2- | LVDS | O | LVDS primary channel differential pair 2 negative signal |
| 10 | | LCD_D3 | TTL | O | LCD Pixel Data bit 3 |
| 11 | | LVDS_A2+ | LVDS | O | LVDS primary channel differential pair 2 positive signal |
| 12 | | GND | GND | P | Ground |
| 13 | | GND | GND | P | Ground |
| 14 | | LCD_D4 | TTL | O | LCD Pixel Data bit 4 |
| 15 | | LVDS_A3- | LVDS | O | LVDS primary channel differential pair 3 negative signal |
| 16 | | LCD_D5 | TTL | O | LCD Pixel Data bit 5 |

| Pin # | EDM | Signal | V | I/O | Description |
|---|---|---|---|---|---|
| 17 | | LVDS_A3+ | LVDS | O | LVDS primary channel differential pair 3 positive signal |
| 18 | | GND | GND | P | Ground |
| 19 | | GND | GND | P | Ground |
| 20 | | LCD_D6 | TTL | O | LCD Pixel Data bit 6 |
| 21 | | LVDS_ACLK- | LVDS | O | LVDS primary channel clock negative signal |
| 22 | | LCD_D7 | TTL | O | LCD Pixel Data bit 7 |
| 23 | | LVDS_ACLK+ | LVDS | O | LVDS primary channel clock positive signal |
| 24 | | GND | GND | P | Ground |
| 25 | | GND | GND | P | Ground |
| 26 | | LCD_D8 | TTL | O | LCD Pixel Data bit 8 |
| 27 | | LVDS_ABL_CTRL | CMOS 3.3V | O | LVDS primary channel panel backlight control |
| 28 | | LCD_D9 | TTL | O | LCD Pixel Data bit 9 |
| 29 | | LVDS_AEN | CMOS 3.3V | O | LVDS primary channel panel backlight enable |
| 30 | | GND | GND | P | Ground |
| 31 | | LVDS_AVDD_EN | CMOS 3.3V | O | LVDS primary channel panel power enable |
| 32 | | LCD_D10 | TTL | O | LCD Pixel Data bit 10 |
| 33 | NC | eDP0_SELFTEST | CMOS 3.3V | I | Embedded Display Port Detection pin |
| 34 | | LCD_D11 | TTL | O | LCD Pixel Data bit 11 |
| 35 | NC | eDP0_HPD | CMOS 3.3V | I | Embedded Display Port Hot Plug Detection pin |
| 36 | | LCD_D12 | TTL | O | LCD Pixel Data bit 12 |
| 37 | | I2C_SDA | CMOS 3.3V | I/O | Display ID DDC data line used for LVDS flat panel detection. If not used this can be assigned to General Purpose $I^2C$ bus data line |
| 38 | | LCD_D13 | TTL | O | LCD Pixel Data bit 13 |
| 39 | | I2C_SCL | CMOS 3.3V | I/O | Display ID DDC clock line used for LVDS flat panel detection. If not used this can be assigned to General Purpose $I^2C$ bus clock line |
| 40 | | LCD_D14 | TTL | O | LCD Pixel Data bit 14 |
| 41 | | GND | GND | P | Ground |
| 42 | | GND | GND | P | Ground |
| 43 | | HDMI1_CLK+ | HDMI | O | HDMI differential pair clock positive signal |
| 44 | | LCD_D15 | TTL | O | LCD Pixel Data bit 15 |
| 45 | | HDMI1_CLK- | HDMI | O | HDMI differential pair clock negative signal |
| 46 | | LCD_D16 | TTL | O | LCD Pixel Data bit 16 |
| 47 | | GND | GND | P | Ground |
| 48 | | GND | GND | P | Ground |
| 49 | | HDMI1_D0+ | HDMI | O | HDMI differential pair 0 positive signal |
| 50 | | LCD_D17 | TTL | O | LCD Pixel Data bit 17 |
| 51 | | HDMI1_D0- | HDMI | O | HDMI differential pair 0 negative signal |
| 52 | | LCD_D18 | TTL | O | LCD Pixel Data bit 18 |
| 53 | | GND | GND | P | Ground |
| 54 | | GND | GND | P | Ground |
| 55 | | HDMI1_D1+ | HDMI | O | HDMI differential pair 1 positive signal |
| 56 | | LCD_D19 | TTL | O | LCD Pixel Data bit 19 |
| 57 | | HDMI1_D1- | HDMI | O | HDMI differential pair 1 negative signal |

| Pin # | EDM | Signal | V | I/O | Description |
|---|---|---|---|---|---|
| 58 | | LCD_D20 | TTL | O | LCD Pixel Data bit 20 |
| 59 | | GND | GND | P | Ground |
| 60 | | GND | GND | P | Ground |
| 61 | | HDMI1_D2+ | HDMI | O | HDMI differential pair 2 positive signal |
| 62 | | LCD_D21 | TTL | O | LCD Pixel Data bit 21 |
| 63 | | HDMI1_D2- | HDMI | O | HDMI differential pair 2 negative signal |
| 64 | | LCD_D22 | TTL | O | LCD Pixel Data bit 22 |
| 65 | | GND | GND | P | Ground |
| 66 | | GND | GND | P | Ground |
| 67 | | HDMI1_HPD<br>DP1_HPD | CMOS 3.3V | I | HDMI/DP Hot plug detection signal that serves as an interrupt request |
| 68 | | LCD_D23 | TTL | O | LCD Pixel Data bit 23 |
| 69 | NC | HDMI1_CAD | HDMI | I / O | Cable Adaptor Detect |
| 70 | | LCD_CLK | TTL | O | LCD Pixel Clock |
| 71 | | HDMI1_CEC | HDMI | I / O | HDMI Consumer Electronics Control |
| 72 | | LCD_HSYNC | TTL | O | LCD Horizontal Synchronization |
| 73 | | I2C_SCL | CMOS 5V | I/O | Display ID DDC data line used for HDMI detection. If not used this can be assigned to General Purpose $I^2C$ bus clock line |
| 74 | | LCD_VSYNC | TTL | O | LCD Vertical Synchronization |
| 75 | | I2C_SDA | CMOS 5V | I/O | Display ID DDC data line used for HDMI detection. If not used this can be assigned to General Purpose $I^2C$ bus data line |
| 76 | | LCD_ BKLEN | TTL | O | LCD backlight control |
| 77 | | GND | GND | P | Ground |
| 78 | | LCD_DRD Y | TTL | O | LCD dot enable pin signal |
| 79 | | PCIEB_CLK+ | PCIE | O | PCI Express channel B clock differential pair positive signal |
| 80 | | LCD_VDDEN | TTL | O | LCD Voltage On |
| 81 | | PCIEB_CLK- | PCIE | O | PCI Express channel B clock differential pair negative signal |
| 82 | | LCD_CNTRST | TTL | O | LCD Backlight Control |
| 83 | | GND | GND | P | Ground |
| 84 | | RSVD | | | Reserved |
| 85 | | PCIEA_CLK+ | PCIE | O | PCI Express channel A clock differential pair positive signal |
| 86 | | GPMC_nCSA | CMOS 3.3V | O | GPMC Chip Select bit A |
| 87 | | PCIEA_CLK- | PCIE | O | PCI Express channel A clock differential pair negative signal |
| 88 | | GND | GND | P | Ground |
| 89 | | GND | GND | P | Ground |
| 90 | | GPMC_nCSB | CMOS 3.3V | O | GPMC Chip Select bit B |
| 91 | | PCIEA_TX+ | PCIE | O | PCI Express channel A Transmit output differential pair positive signal |
| 92 | | GPMC_nCSC | CMOS 3.3V | O | GPMC Chip Select bit C |
| 93 | | PCIEA_TX- | PCIE | O | PCI Express channel A Transmit output differential pair negative signal |
| 94 | NC | GND | GND | P | Ground |
| 95 | | GND | GND | P | Ground |
| 96 | | GPMC_nCSD | CMOS 3.3V | O | GPMC Chip Select bit D |

| Pin # | EDM | Signal | V | I/O | Description |
|---|---|---|---|---|---|
| 97 | | PCIEA_RX+ | PCIE | I | PCI Express channel A Receive input differential pair positive signal |
| 98 | | GPMC_nCSE | CMOS 3.3V | O | GPMC Chip Select bit E |
| 99 | | PCIEA_RX- | PCIE | I | PCI Express channel A Receive input differential pair negative signal |
| 100 | | GND | GND | P | Ground |
| 101 | | GND | GND | P | Ground |
| 102 | | GPMC_WAIT | CMOS 3.3V | I | External indication of wait |
| 103 | | PCIEB_TX+ | PCIE | O | PCI Express channel B Transmit output differential pair positive signal |
| 104 | | GPMC_WP | CMOS 3.3V | O | GPMC Write Protect / Enable |
| 105 | | PCIEB_TX- | PCIE | O | PCI Express channel B Transmit output differential pair negative signal |
| 106 | | GPMC_CLE | CMOS 3.3V | O | GPMC Lower Byte Enable. Also used for Command Latch Enable |
| 107 | NC | PCIE_PRST# | PCIE | I | PCI Express interface presence detection pin |
| 108 | | GPMC_ALE | CMOS 3.3V | O | GPMC Address Valid or Address Latch Enable |
| 109 | | PCIEB_RX+ | PCIE | I | PCI Express channel B Receive input differential pair positive signal |
| 110 | | GPMC_WE | CMOS 3.3V | I | GPMC Write Enable |
| 111 | | PCIEB_RX- | PCIE | I | PCI Express channel B Receive input differential pair negative signal |
| 112 | | GPMC_RE | CMOS 3.3V | O | GPMC Read Enable |
| 113 | | PCIECLK_OEA | PCIE | O | PCI Express channel A hot plug detection signal |
| 114 | NC | RSVD | | | Reserved |
| 115 | | PCIECLK_OEB | PCIE | O | PCI Express channel B hot plug detection signal |
| 116 | | GPMC_A10 | CMOS 3.3V | O | GPMC output address bit 10 |
| 117 | | PCIE_WAKE# | CMOS 3.3V | I | PCI Express Wake Event: Sideband wake signal asserted by components requesting wake up |
| 118 | | GPMC_A9 | CMOS 3.3V | O | GPMC output address bit 9 |
| 119 | | PCIE_RST# | CMOS 3.3V | O | PCI Express Reset signal for external devices |
| 120 | | GPMC_A8 | CMOS 3.3V | O | GPMC output address bit 8 |
| 121 | | GND | GND | P | Ground |
| 122 | | GPMC_A7 | CMOS 3.3V | O | GPMC output address bit 7 |
| 123 | | SATA1_RXP | SATA | I | Serial ATA channel 1 Receive differential pair positive signal |
| 124 | | GND | GND | P | Ground |
| 125 | | SATA1_RXN | SATA | I | Serial ATA channel 1 Receive differential pair negative signal |
| 126 | | KEY | | | |
| 127 | | KEY | | | |
| 128 | | KEY | | | |
| 129 | | KEY | | | |

| Pin # | EDM | Signal | V | I/O | Description |
|---|---|---|---|---|---|
| 130 | | KEY | | | |
| 131 | | KEY | | | |
| 132 | | KEY | | | |
| 133 | NC | SATA1_nACT | SATA | I/O | Serial ATA LED. Open collector output pin driven during SATA command activity |
| 134 | | GPMC_A6 | CMOS 3.3V | O | GPMC output address bit 6 |
| 135 | | SATA1_TXP | SATA | O | Serial ATA channel 1 Transmit differential pair positive signal |
| 136 | | GPMC_A5 | CMOS 3.3V | O | GPMC output address bit 5 |
| 137 | | SATA1_TXN | SATA | O | Serial ATA channel 1 Transmit differential pair negative signal |
| 138 | | GPMC_A4 | CMOS 3.3V | O | GPMC output address bit 4 |
| 139 | | USB1_HUB_RST | USB | O | Universal Serial Bus carrier board hub reset pin |
| 140 | | GPMC_A3 | CMOS 3.3V | O | GPMC output address bit 3 |
| 141 | | USB2_OC | CMOS 3.3V | I | Over current detect input pin to monitor USB power over current |
| 142 | | GPMC_A2 | CMOS 3.3V | O | GPMC output address bit 2 |
| 143 | | StdB2_SSRX+ | USB | I | Universal Serial Bus Superspeed receiver differential pair positive signal |
| 144 | | GPMC_A1 | CMOS 3.3V | O | GPMC output address bit 1 |
| 145 | | StdB2_SSRX- | USB | I | Universal Serial Bus Superspeed receiver differential pair negative signal |
| 146 | | GPMC_D15 | CMOS 3.3V | I/O | GPMC data bit 15 |
| 147 | | GND2_DRAIN | USB | P | Universal Serial Bus ground for signal return |
| 148 | | GND | GND | P | Ground |
| 149 | | StdB2_SSTX+ | USB | O | Universal Serial Bus Superspeed transmitter differential pair positive signal |
| 150 | | GPMC_D14 | CMOS 3.3V | I/O | GPMC data bit 14 |
| 151 | | StdB2_SSTX- | USB | O | Universal Serial Bus Superspeed transmitter differential pair negative signal |
| 152 | | GPMC_D13 | CMOS 3.3V | I/O | GPMC data bit 13 |
| 153 | | GND | GND | P | Ground |
| 154 | | GND | GND | P | Ground |
| 155 | | USB2_OTG_ID | USB | I | Universal Serial Bus On-The-Go detection signal |
| 156 | | GPMC_D12 | CMOS 3.3V | I/O | GPMC data bit 12 |
| 157 | | USB2_D+ | USB | I/O | Universal Serial Bus port 2 differential pair positive signal |
| 158 | | GPMC_D11 | CMOS 3.3V | I/O | GPMC data bit 11 |
| 159 | | USB2_D- | USB | I/O | Universal Serial Bus port 2 differential pair negative signal |

| Pin # | EDM | Signal | V | I/O | Description |
|---|---|---|---|---|---|
| 160 | | GPMC_D10 | CMOS 3.3V | I/O | GPMC data bit 10 |
| 161 | | USB2_VBUS | 5V | I/O | Universal Serial Bus port 2 power |
| 162 | | GPMC_D9 | CMOS 3.3V | I/O | GPMC data bit 9 |
| 163 | | USB2_PWR_EN | USB | O | Universal Serial Bus power enable |
| 164 | | GPMC_D8 | CMOS 3.3V | I/O | GPMC data bit 8 |
| 165 | | USB1_OC | CMOS 3.3V | I | Over current detect input pin to monitor USB power over current |
| 166 | | GND | GND | P | Ground |
| 167 | | StdB1_SSRX+ | USB | I | Universal Serial Bus Superspeed receiver differential pair positive signal |
| 168 | | GPMC_D7 | CMOS 3.3V | I/O | GPMC data bit 7 |
| 169 | | StdB1_SSRX- | USB | I | Universal Serial Bus Superspeed receiver differential pair negative signal |
| 170 | | GPMC_D6 | CMOS 3.3V | I/O | GPMC data bit 6 |
| 171 | | GND1_DRAIN | USB | P | Universal Serial Bus ground for signal return |
| 172 | | GPMC_D5 | CMOS 3.3V | I/O | GPMC data bit 5 |
| 173 | | StdB1_SSTX+ | USB | O | Universal Serial Bus Superspeed transmitter differential pair positive signal |
| 174 | | GPMC_D4 | CMOS 3.3V | I/O | GPMC data bit 4 |
| 175 | | StdB1_SSTX- | USB | O | Universal Serial Bus Superspeed transmitter differential pair negative signal |
| 176 | | GPMC_D3 | CMOS 3.3V | I/O | GPMC data bit 3 |
| 177 | | GND | GND | P | Ground |
| 178 | | GPMC_D2 | CMOS 3.3V | I/O | GPMC data bit 2 |
| 179 | | USB1_D- | USB | I/O | Universal Serial Bus port 1 differential pair negative signal |
| 180 | | GPMC_D1 | CMOS 3.3V | I/O | GPMC data bit 1 |
| 181 | | USB1_D+ | USB | I/O | Universal Serial Bus port 1 differential pair positive signal |
| 182 | | GPMC_D0 | CMOS 3.3V | I/O | GPMC data bit 0 |
| 183 | | USB1_VBUS | 5V | I/O | Universal Serial Bus port 1 power |
| 184 | | GND | GND | P | Ground |
| 185 | | GND | GND | P | Ground |
| 186 | | I2S2_RXD | CMOS 3.3V | I | Secondary Integrated Interchip Sound ($I^2S$) channel receive data line |
| 187 | | I2S1_RXD | CMOS 3.3V | I | Primary Integrated Interchip Sound ($I^2S$) channel receive data line |
| 188 | | I2S2_TXFS | CMOS 3.3V | O | Secondary Integrated Interchip Sound ($I^2S$) channel frame synchronization signal |
| 189 | | I2S1_TXFS | CMOS 3.3V | O | Primary Integrated Interchip Sound ($I^2S$) channel frame synchronization signal |

| Pin # | EDM | Signal | V | I/O | Description |
|---|---|---|---|---|---|
| 190 | | I2S2_TXD | CMOS 3.3V | O | Secondary Integrated Interchip Sound ($I^2S$) channel transmit data line |
| 191 | | I2S1_TXD | CMOS 3.3V | O | Primary Integrated Interchip Sound ($I^2S$) channel transmit data line |
| 192 | | I2S2_TXC | CMOS 3.3V | O | Secondary Integrated Interchip Sound ($I^2S$) channel word clock signal |
| 193 | | I2S1_TXC | CMOS 3.3V | O | Primary Integrated Interchip Sound ($I^2S$) channel word clock signal |
| 194 | | I2S2_CLK | CMOS 3.3V | O | Secondary Integrated Interchip Sound ($I^2S$) channel master clock signal |
| 195 | | I2S1_CLK | CMOS 3.3V | O | Primary Integrated Interchip Sound ($I^2S$) channel master clock signal |
| 196 | | SPDIF_OUT | SPDIF | O | Sony / Philips Digital Interconnect Format Audio output |
| 197 | | CAN2+ | CAN | I/O | Secondary CAN (controller Area Network) differential pair positive signal |
| 198 | | GND | GND | P | Ground |
| 199 | | CAN2- | CAN | I/O | Secondary CAN (controller Area Network) differential pair negative signal |
| 200 | | CAN1+ | CAN | I/O | Primary CAN (controller Area Network) differential pair positive signal |
| 201 | | GND | GND | P | Ground |
| 202 | | CAN1- | CAN | I/O | Primary CAN (controller Area Network) differential pair negative signal |
| 203 | | SDIO_CD | CMOS 3.3V | I/O | MMC/SDIO Card Detect |
| 204 | | GND | GND | P | Ground |
| 205 | | SDIO_CMD | CMOS 3.3V | I/O | MMC/SDIO Command |
| 206 | | SDIO_CLK | CMOS 3.3V | O | MMC/SDIO Clock |
| 207 | | SDIO_WP | CMOS 3.3V | I/O | MMC/SDIO Write Protect |
| 208 | NC | SDIO_LED | CMOS 3.3V | O | MMC/SDIO LED |
| 209 | | SDIO_DAT1 | CMOS 3.3V | I/O | MMC/SDIO Data bit 1 |
| 210 | | SDIO_PWR | CMOS 3.3V | O | MMC/SDIO Power Enable |
| 211 | | SDIO_DAT3 | CMOS 3.3V | I/O | MMC/SDIO Data bit 3 |
| 212 | | SDIO_DAT0 | CMOS 3.3V | I/O | MMC/SDIO Data bit 0 |
| 213 | NC | SDIO_DAT5 | CMOS 3.3V | I/O | MMC/SDIO Data bit 5 |
| 214 | | SDIO_DAT2 | CMOS 3.3V | I/O | MMC/SDIO Data bit 2 |
| 215 | NC | SDIO_DAT7 | CMOS 3.3V | I/O | MMC/SDIO Data bit 7 |
| 216 | NC | SDIO_DAT4 | CMOS 3.3V | I/O | MMC/SDIO Data bit 4 |
| 217 | | GND | GND | P | Ground |
| 218 | NC | SDIO_DAT6 | CMOS 3.3V | I/O | MMC/SDIO Data bit 6 |

| Pin # | EDM | Signal | V | I/O | Description |
|---|---|---|---|---|---|
| 219 | | SPI2_MOSI | CMOS 3.3V | O | Serial Peripheral Interface primary channel master output slave input signal |
| 220 | | GND | GND | P | Ground |
| 221 | | SPI2_MISO | CMOS 3.3V | I | Serial Peripheral Interface primary channel master input slave output signal |
| 222 | | SPI1_MOSI | CMOS 3.3V | O | Serial Peripheral Interface secondary channel master output slave input signal |
| 223 | | SPI2_CLK | CMOS 3.3V | O | Serial Peripheral Interface primary channel clock signal |
| 224 | | SPI1_MISO | CMOS 3.3V | I | Serial Peripheral Interface secondary channel master input slave output signal |
| 225 | | SPI2_CS0 | CMOS 3.3V | O | Serial Peripheral Interface primary channel Chip Select 0 signal |
| 226 | | SPI1_CLK | CMOS 3.3V | O | Serial Peripheral Interface secondary channel clock signal |
| 227 | NC | SPI2_CS1 | CMOS 3.3V | O | Serial Peripheral Interface primary channel Chip Select 1 signal. Do not use if only 1 SPI device is used |
| 228 | | SPI1_CS0 | CMOS 3.3V | O | Serial Peripheral Interface secondary channel Chip Select 0 signal |
| 229 | | GND | GND | P | Ground |
| 230 | | SPI1_CS1 | CMOS 3.3V | O | Serial Peripheral Interface secondary channel Chip Select 1 signal. Do not use if only 1 SPI device is used |
| 231 | | I2C2_SCL | CMOS 3.3V | I/O | $I^2C$ bus clock line |
| 232 | | GND | GND | P | Ground |
| 233 | | I2C2_SDA | CMOS 3.3V | I/O | $I^2C$ bus data line |
| 234 | | UART2_CTS | UART | O | Universal Asynchronous Receive Transmit secondary channel clear to send signal |
| 235 | | I2C3_SCL | CMOS 3.3V | I/O | $I^2C$ bus clock line |
| 236 | | UART2_TXD | UART | O | Universal Asynchronous Receive Transmit secondary channel transmit data signal |
| 237 | | I2C3_SDA | CMOS 3.3V | I/O | $I^2C$ bus data line |
| 238 | | UART2_RXD | UART | I | Universal Asynchronous Receive Transmit secondary channel receive data signal |
| 239 | | GND | GND | P | Ground |
| 240 | | UART2_RTS | UART | O | Universal Asynchronous Receive Transmit secondary channel request to send signal |
| 241 | | UART1_CTS | UART | O | Universal Asynchronous Receive Transmit secondary channel clear to send signal |
| 242 | | UART2_DCD | UART | I | Universal Asynchronous Receive Transmit secondary channel carrier detect signal |

| Pin # | EDM | Signal | V | I/O | Description |
|---|---|---|---|---|---|
| 243 | | UART1_TXD | UART | O | Universal Asynchronous Receive Transmit secondary channel transmit data signal |
| 244 | | UART2_DSR | UART | I | Universal Asynchronous Receive Transmit secondary channel data set ready signal |
| 245 | | UART1_RXD | UART | I | Universal Asynchronous Receive Transmit secondary channel receive data signal |
| 246 | | UART2_DTR | UART | O | Universal Asynchronous Receive Transmit secondary channel data terminal ready signal |
| 247 | | UART1_RTS | UART | O | Universal Asynchronous Receive Transmit secondary channel request to send signal |
| 248 | | UART2_RI | UART | I | Universal Asynchronous Receive Transmit secondary channel ring indication signal |
| 249 | | GND | GND | P | Ground |
| 250 | | GND | GND | P | Ground |
| 251 | NC | S3 | CMOS 3.3V | O | S3 signal shuts off power to all runtime system components that are not maintained during S3 state (suspend to RAM) |
| 252 | | ON/OFF | CMOS 3.3V | I | Power ON button input signal |
| 253 | NC | S5 | CMOS 3.3V | O | S5 signal shuts off power to the system. Restart is only possible with power button or by a system wake up event |
| 254 | | RESET | CMOS 3.3V | I | Reset button input signal |
| 255 | | GPIO | CMOS 3.3V | I/O | General Purpose Input Output |
| 256 | | GPIO | CMOS 3.3V | I/O | General Purpose Input Output |
| 257 | | GPIO | CMOS 3.3V | I/O | General Purpose Input Output |
| 258 | | GPIO | CMOS 3.3V | I/O | General Purpose Input Output |
| 259 | | GPIO | CMOS 3.3V | I/O | General Purpose Input Output |
| 260 | | GPIO | CMOS 3.3V | I/O | General Purpose Input Output |
| 261 | | GPIO | CMOS 3.3V | I/O | General Purpose Input Output |
| 262 | | GPIO | CMOS 3.3V | I/O | General Purpose Input Output |
| 263 | | GPIO | CMOS 3.3V | I/O | General Purpose Input Output |
| 264 | | GPIO | CMOS 3.3V | I/O | General Purpose Input Output |
| 265 | | GND | GND | P | Ground |
| 266 | | GND | GND | P | Ground |
| 267 | | RSVD | | | Reserved |
| 268 | | RSVD | | | Reserved |
| 269 | | RSVD | | | Reserved |
| 270 | | RSVD | | | Reserved |

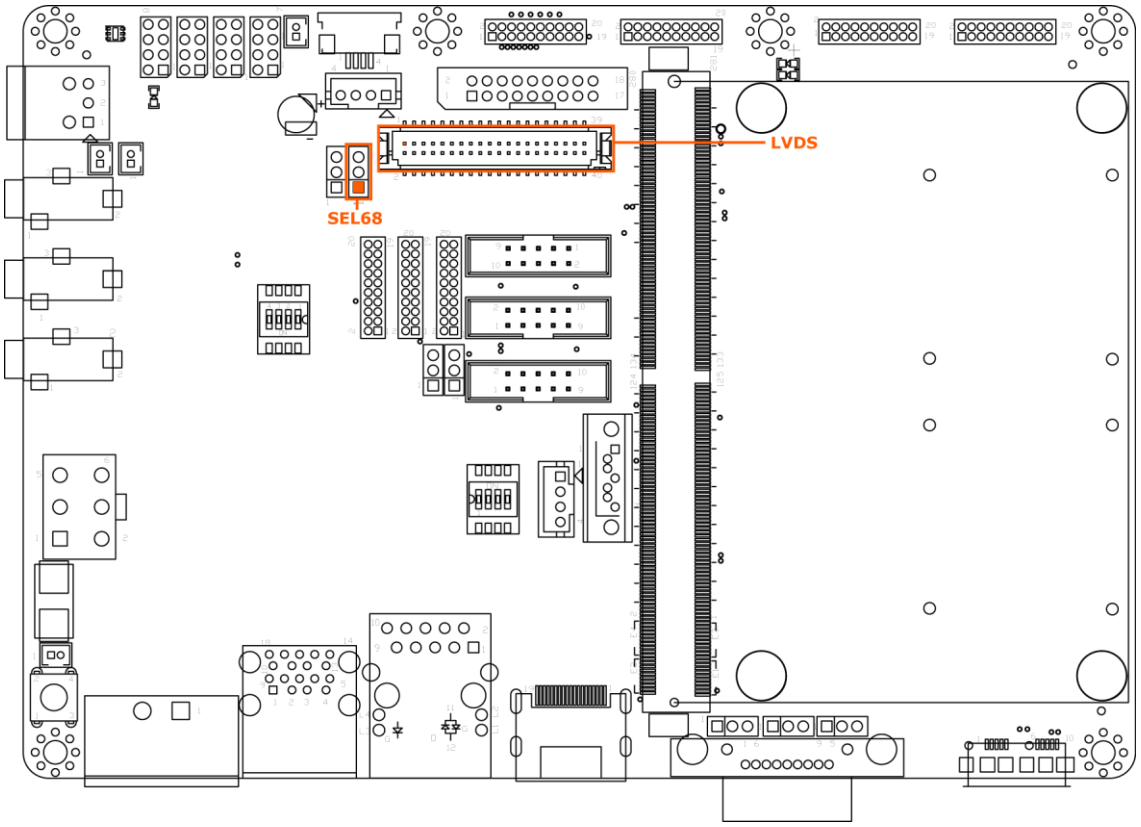
| Pin # | EDM | Signal | V | I/O | Description |
|---|---|---|---|---|---|
| 271 | | RSVD | | | Reserved |
| 272 | | RSVD | | | Reserved |
| 273 | | RSVD | | | Reserved |
| 274 | | RSVD | | | Reserved |
| 275 | | RSVD | | | Reserved |
| 276 | | RSVD | | | Reserved |
| 277 | | RSVD | | | Reserved |
| 278 | | RSVD | | | Reserved |
| 279 | | Watchdog | CMOS 3.3V | O | Watchdog event indication signal |
| 280 | | RSVD | | | Reserved |
| 281 | | VCC_RTC | 3.3V | I | Input power for RTC clock |

## 6.2. LVDS Connector

EDM type 1 modules in the carrier board provide up to one single-channel LVDS which is defined as LVDS_A. Systems normally use a single-channel LVDS for most displays.

Each EDM LVDS channel consists of four differential data pairs and a differential clock pair for a total of five differential pairs per channel. Certain EDM module processors or chipsets may not use all pairs.

There are five single-ended signals included to support the LVDS interface: two lines are used for an $I^2C$ interface that may be used to support EDID or other panel information and identification schemes. Additionally, there are an LVDS power enable (LVDS_xVDD_EN) and backlight control and enable lines (LVDS_xBL_CTRL and LVDS_xEN).




| | SEL68 |
|---|---|
| High | 1-2 |
| Low | 2-3 |

**Table 2: 6 or 8 bit panels can also be set with the jumper (SEL68)**

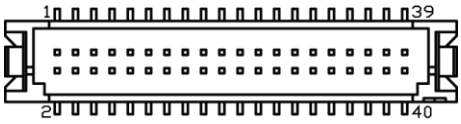



**Figure 23 - LVDS Connector (for example: Hirose DF13-40DP-1.25)**

| Pin # | Signal | Description | Pin # | Signal | Description |
|---|---|---|---|---|---|
| 1 | 12V | 12V power to data driver circuit | 2 | 5V | 5V power to data driver circuit |
| 3 | 12V | | 4 | 5V | |
| 5 | LCD_ENB | LCD on/off @ 5V | 6 | PWM_5V | Backlight PWM @ 5V |
| 7 | LCD_ENBK | LCD on/off @ 3.3V | 8 | PWM_3.3V | Backlight PWM @ 3.3V |
| 9 | GND | Ground | 10 | GND | Ground |
| 11 | SEL68 | LVDS 18/24 bit selection pin | 12 | 3.3V | 3.3V power to data driver circuit |
| 13 | LVDS_D0- | LVDS primary channel differential pair 0 signal | 14 | 3.3V | |
| 15 | LVDS_D0+ | | 16 | LVDS REV | LVDS Reverse Scan signal |
| 17 | GND | Ground | 18 | LVDS R/L | Horizontal Reverse Scan Control |
| 19 | LVDS_D1- | LVDS primary channel differential pair 1 signal | 20 | LVDS U/D | Vertical Reverse Scan Control |
| 21 | LVDS_D1+ | | 22 | SCL | Display ID DDC clock line used for LVDS flat panel detection |
| 23 | GND | Ground | 24 | SDA | Display ID DDC data line used for LVDS flat panel detection. |
| 25 | LVDS_D2- | LVDS primary channel differential pair 2 signal | 26 | LED enable | Backlight on/off |
| 27 | LVDS_D2+ | | 28 | LED+ | Backlight LED signals (5V) |
| 29 | GND | Ground | 30 | LED+ | |
| 31 | LVDS_CLK- | LVDS primary channel differential pair clock signal | 32 | LED+ | |
| 33 | LVDS_CLK+ | | 34 | LVDS enable | LCD signal (driver IC) on/off |
| 35 | GND | Ground | 36 | LED- | Ground return signals for LED backlight signals |
| 37 | LVDS_D3- | LVDS primary channel differential pair 3 signal | 38 | LED- | |
| 39 | LVDS_D3+ | | 40 | LED- | |

**Table 3 - LVDS Connector Pin-out**

## 6.3. HDMI

HDMI provides a digital audio/video interface that connects to a compatible television or monitor.

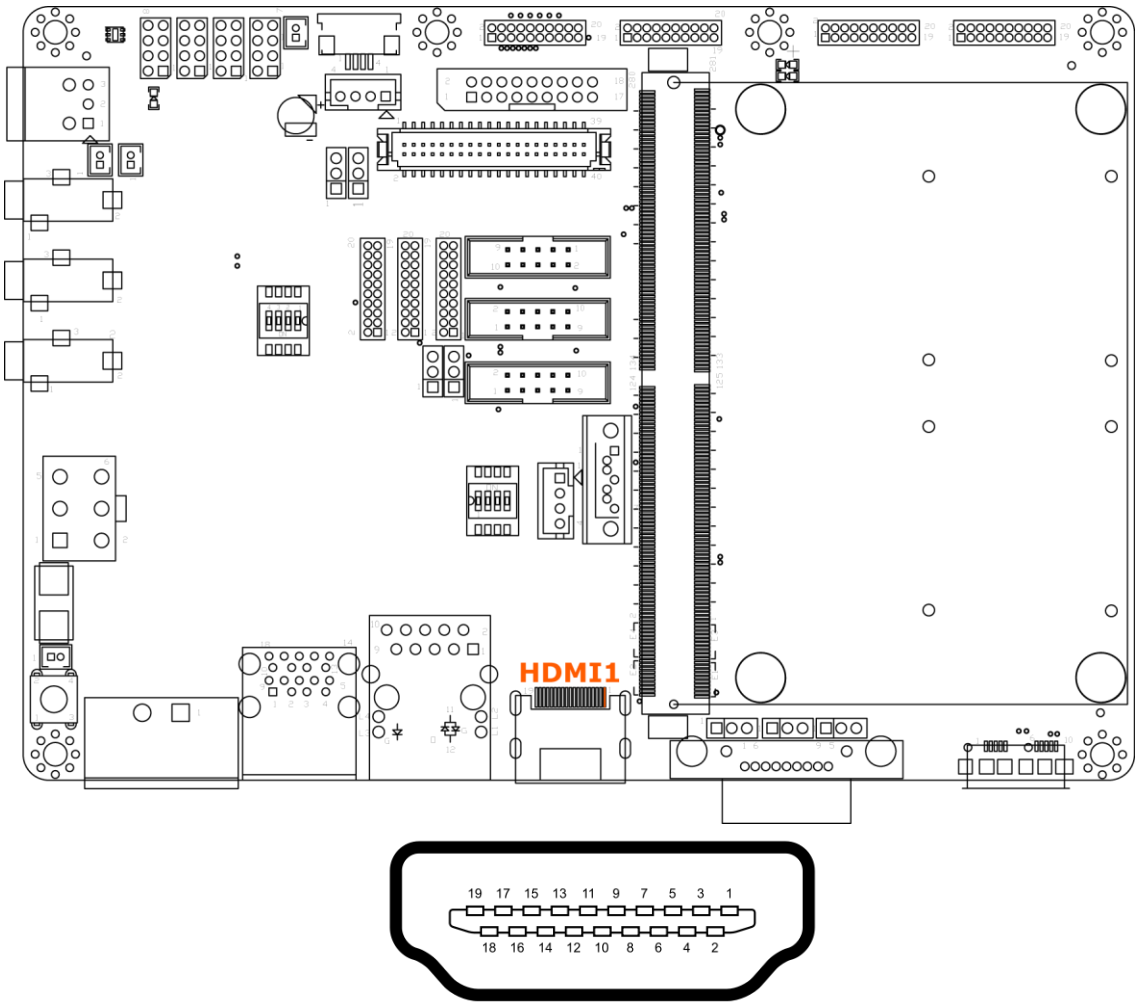


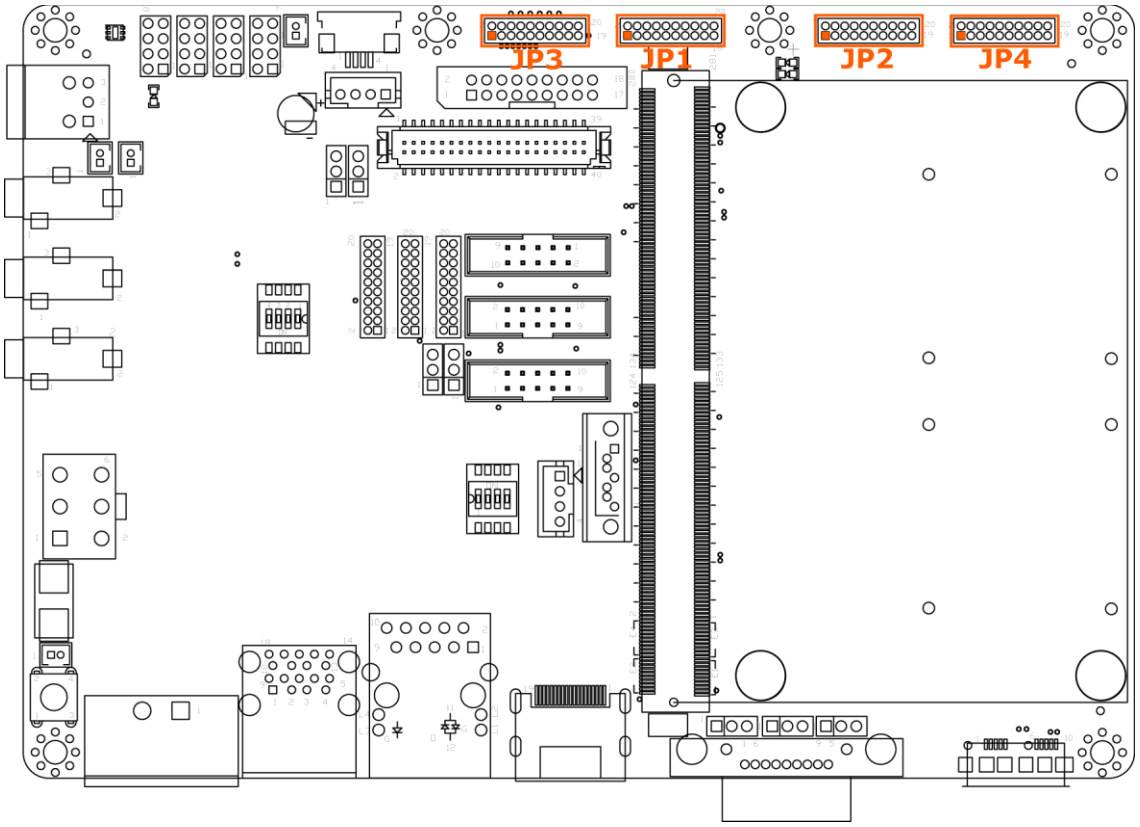

**Figure 24 - HDMI Connector Pin-out**

| Pin # | Signal | Description | Pin # | Signal | Description |
|---|---|---|---|---|---|
| 1 | HDMI_D2+ | HDMI differential pair 2 signal | 2 | Shield_D2 | Shield of data pair 2 |
| 3 | HDMI_D2- | | 4 | HDMI_D1+ | HDMI differential pair 1 signal |
| 5 | Shield_D1 | Shield of data pair 1 | 6 | HDMI_D1- | |
| 7 | HDMI_D0+ | HDMI differential pair 2 signal | 8 | Shield_D0 | Shield of data pair 0 |
| 9 | HDMI_D0- | | 10 | HDMI_CLK+ | HDMI differential clock signal |
| 11 | Shield_CLK | Shield of Clock pair | 12 | HDMI_CLK- | |
| 13 | CEC | Consumer Electronics Control Interface | 14 | RSVD | Reserved |
| 15 | DDC Clock | DDC based control clock signal | 16 | DDC Data | DDC based control data signal |
| 17 | GND | Ground | 18 | +5V | 5V Power |
| 19 | HPD | Hot plug detect | | | |

**Table 4 - HDMI Connector Pin-out**

## 6.4. Expansion headers

The expansion headers are a standardized interface that contains TTL, $I^2C$, SPI, GPIO and power.




| JP3 pin # | Function | JP3 pin # | Function |
|---|---|---|---|
| 1 | +3.3V | 2 | +3.3V |
| 3 | X | 4 | +3.3V |
| 5 | X | 6 | X |
| 7 | X | 8 | X |
| 9 | X | 10 | X |
| 11 | X | 12 | X |
| 13 | X | 14 | X |
| 15 | X | 16 | LVDS_AVDD_EN |
| 17 | X | 18 | GND |
| 19 | GND | 20 | GND |

| JP1 pin # | Function | JP3 pin # | Function |
|---|---|---|---|
| 1 | R_DSS_DATA0 | 2 | R_DSS_DATA10 |
| 3 | R_DSS_DATA1 | 4 | R_DSS_DATA11 |
| 5 | R_DSS_DATA2 | 6 | R_DSS_DATA12 |
| 7 | R_DSS_DATA3 | 8 | R_DSS_DATA13 |
| 9 | R_DSS_DATA4 | 10 | R_DSS_DATA14 |
| 11 | R_DSS_DATA5 | 12 | R_DSS_DATA15 |
| 13 | R_DSS_DATA6 | 14 | R_DSS_DATA16 |
| 15 | R_DSS_DATA7 | 16 | R_DSS_DATA17 |
| 17 | R_DSS_DATA8 | 18 | R_DSS_DATA18 |
| 19 | R_DSS_DATA9 | 20 | R_DSS_DATA19 |

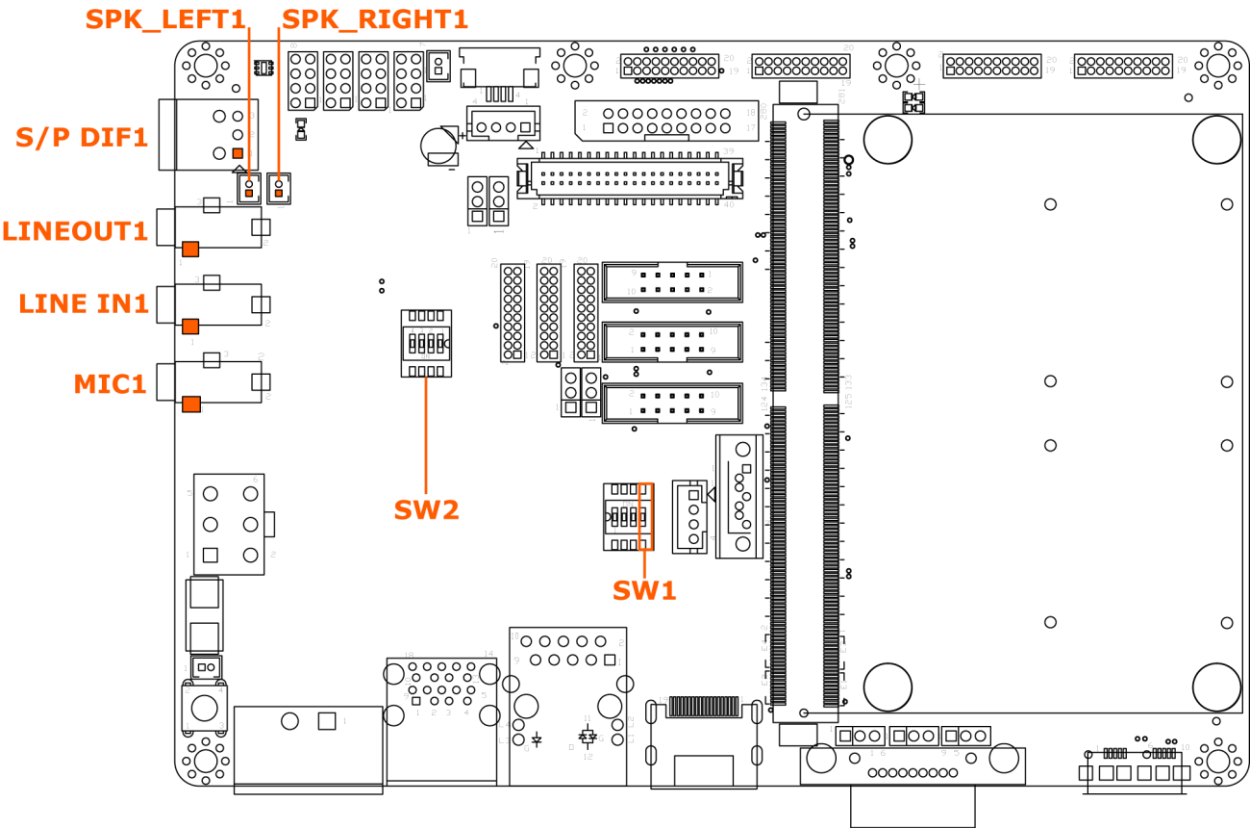
| JP2 pin # | Function | JP3 pin # | Function |
|---|---|---|---|
| 1 | +3.3V | 2 | +3.3V |
| 3 | R_DISP0_CNTRST | 4 | R_DSS_DATA20 |
| 5 | R_DISP0_VDDEN | 6 | R_DSS_DATA21 |
| 7 | $I^2C1\_SDA$ | 8 | R_DSS_DATA22 |
| 9 | $I^2C1\_SCL$ | 10 | R_DSS_DATA23 |
| 11 | $I^2C2\_SDA$ | 12 | R_DSS_PCLK |
| 13 | $I^2C2\_SCL$ | 14 | R_DSS_VSYNC |
| 15 | $I^2C3\_SDA$ | 16 | R_DSS_HSYNC |
| 17 | $I^2C3\_SCL$ | 18 | R_DISP0_DRDY |
| 19 | GND | 20 | GND |

| JP4 pin # | Function | JP3 pin # | Function |
|---|---|---|---|
| 1 | +5V | 2 | +5V |
| 3 | +5V | 4 | GPIO_P256 |
| 5 | +5V | 6 | GPIO_P258 |
| 7 | SPI1_MOSI | 8 | GPIO_P260 |
| 9 | SPI1_MISO | 10 | GPIO_P262 |
| 11 | SPI1_CLK | 12 | GPIO_P264 |
| 13 | SPI1_CS0 | 14 | GPIO_P259 |
| 15 | SPI1_CS1 | 16 | GPIO_P261 |
| 17 | GND | 18 | GPIO_P263 |
| 19 | GND | 20 | GND |

**Table 5 - Expansion header Connector Pin-out (female header 10x2 pitch 1.27 mm)**

## 6.5. Audio

The EDM1 carrier board contains several Audio interfaces, ranging from line in/out , S/P DIF to amplified speakers. The Carrier Board has two audio codec's, each of them can be selected with dipswitch SW1. Next to that the user can also select which $I^2C$ and $I^2S$is used.




| SPK_Left1 | |
|---|---|
| 1 | S_OUTL+ |
| 2 | S_OUTL- |

| SPK_RIGHT1 | |
|---|---|
| 1 | S_OUTR+ |
| 2 | S_OUTR- |

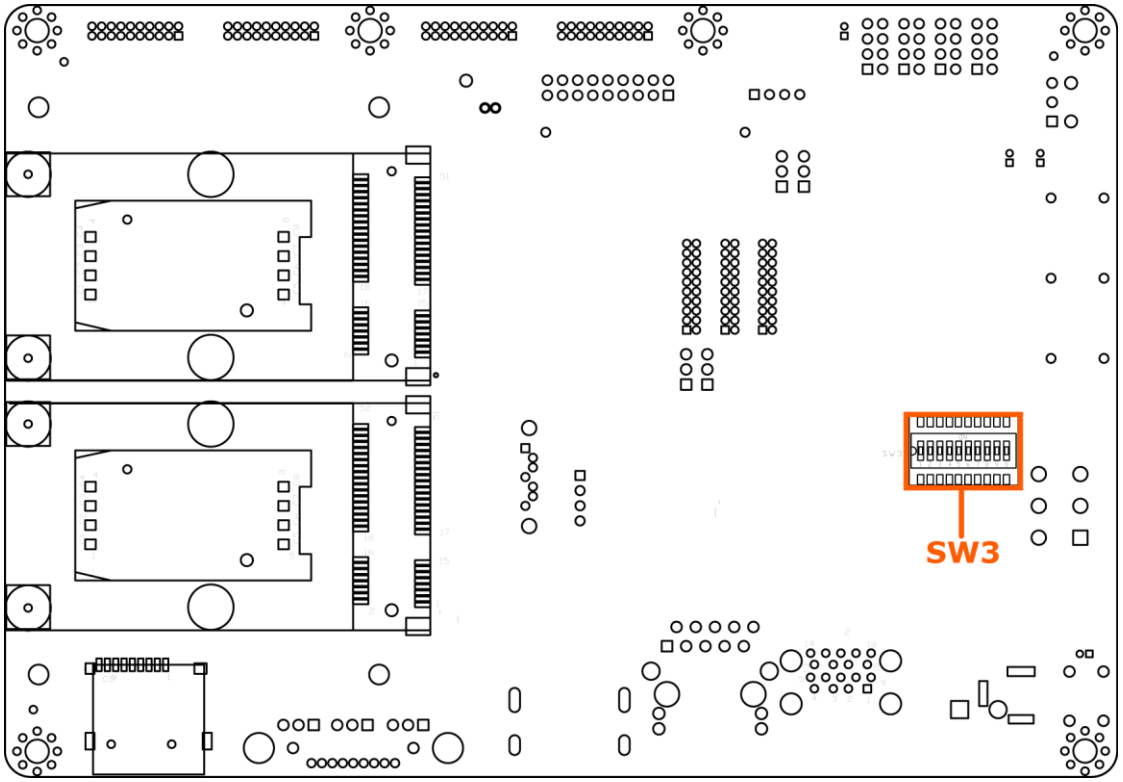
**Table 6 - Speaker connectors Pin-out (wafer 2pin pitch 1.25 mm)**

| SW1 (RS-232/485/422 Select on COM2) | RS-422 | RS-485 | RS-232 |
|---|---|---|---|
| 1 | ON | OFF | OFF |
| 2 | OFF | ON | OFF |
| 3 | OFF | OFF | ON |
| **SW1 (Audio output select)** | **SGTL5000** | **TLV320** | |
| 4 | OFF | ON | |

**Table 7: Selection of audio codec with dipswitch SW1 (4)**

| SW2 (Audio I²C select) | I²C2 | I²C3 | OFF |
|---|---|---|---|
| 1 | ON | OFF | OFF |
| 2 | ON | OFF | OFF |
| 3 | OFF | ON | OFF |
| 4 | OFF | ON | OFF |

**Table 8: Selection of I²C with dipswitch SW2 (1-4)**




| SW3 (Audio I²S select) | SGTL5000 | TLV320 | OFF |
|---|---|---|---|
| 1 | ON | OFF | OFF |
| 2 | ON | OFF | OFF |
| 3 | ON | OFF | OFF |
| 4 | ON | OFF | OFF |
| 5 | ON | OFF | OFF |
| 6 | OFF | ON | OFF |
| 7 | OFF | ON | OFF |
| 8 | OFF | ON | OFF |
| 9 | OFF | ON | OFF |
| 0 | OFF | ON | OFF |

**Table 9: Connect I²S to the selected audio codec with dipswitch SW3 (1-0)**

## 6.6. Gigabit Ethernet

Utilizes the IEEE 802.3 PHY / MDI interface circuit resources between the module and carrier board, with the Ethernet PHY located on the EDM module and the coupling magnetics located on the carrier board.

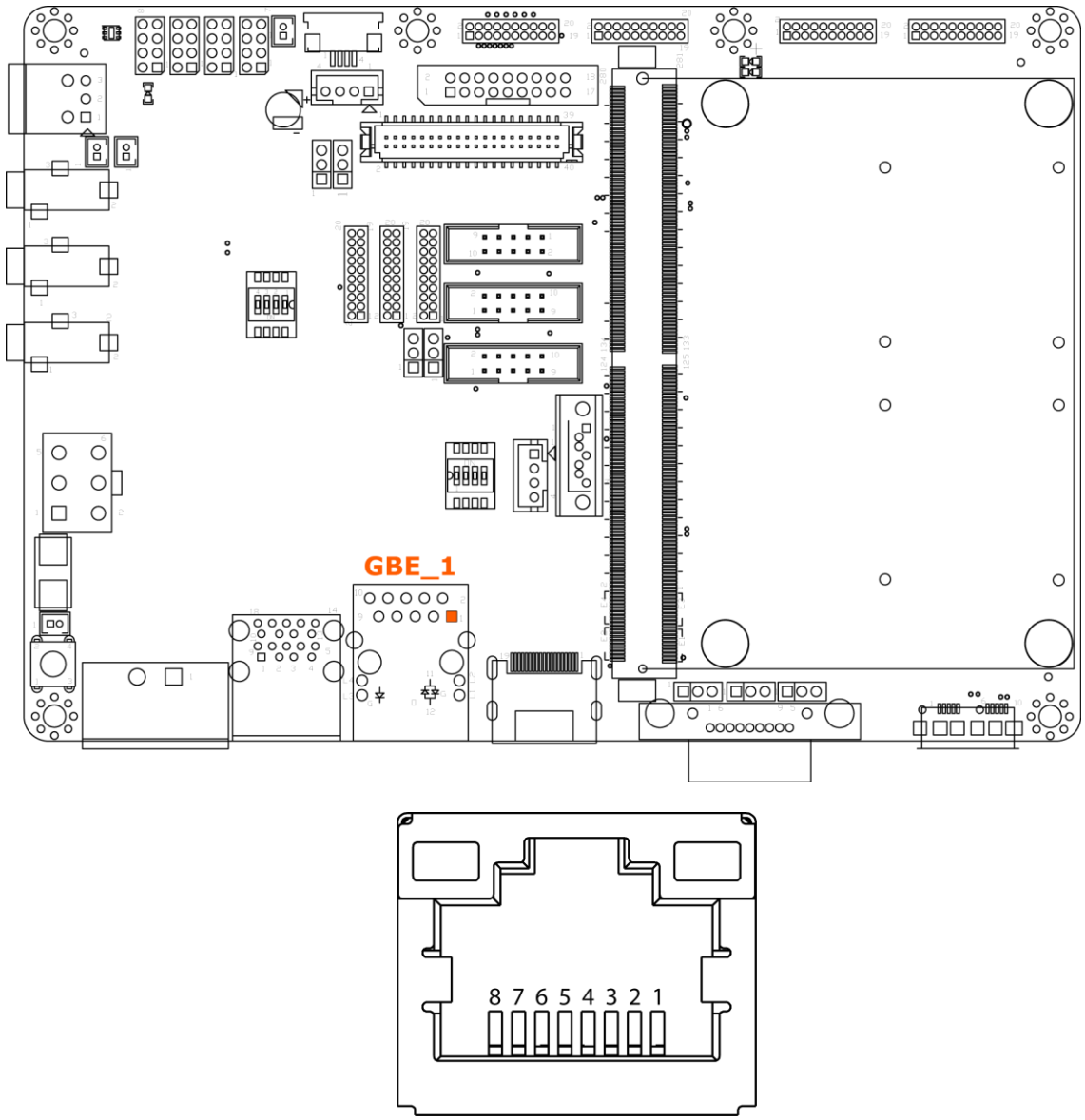


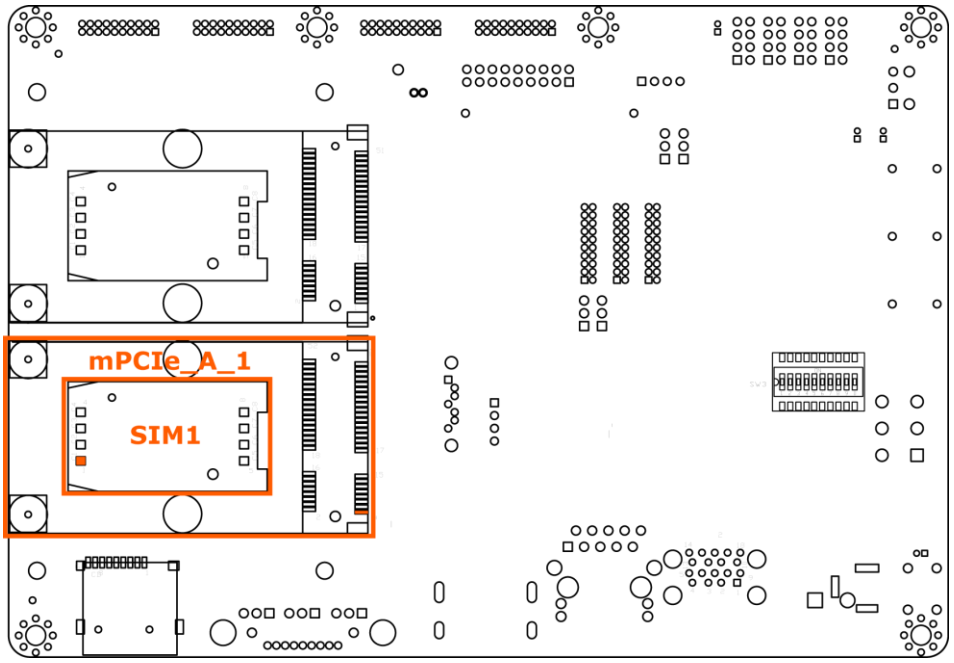

**Figure 25 - Gigabit Ethernet RJ-45 Connector**

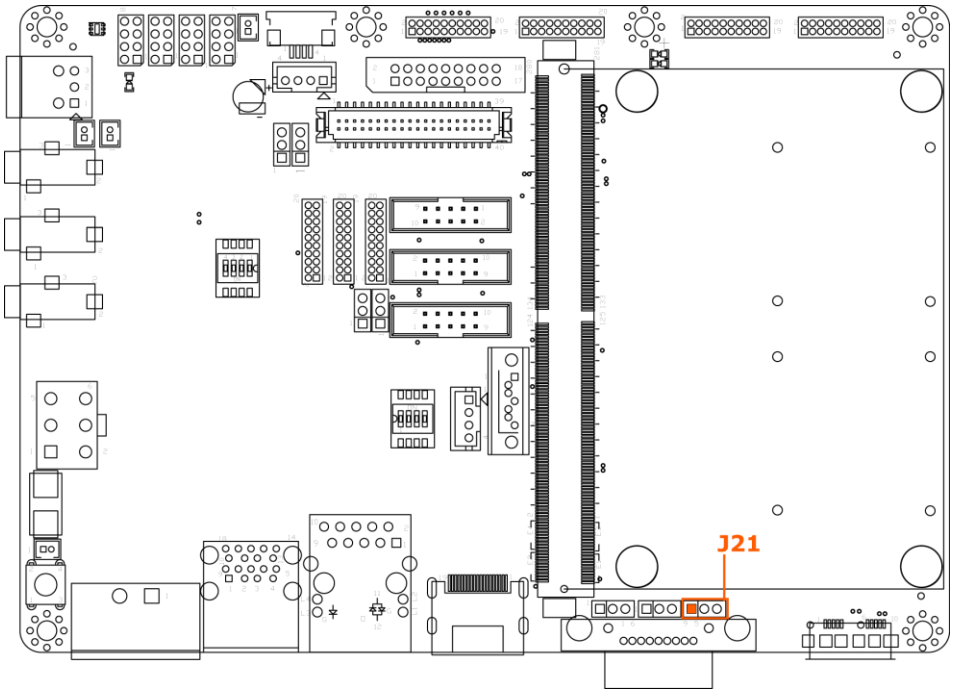
| Pin # | 1000 Mbps | 100 Mbps | 10 Mbps |
|---|---|---|---|
| 1 | MDI0+ | Transmit Data+ | Transmit Data+ |
| 2 | MDI0- | Transmit Data- | Transmit Data- |
| 3 | MDI1+ | Receive Data+ | Receive Data+ |
| 4 | MDI2+ | | |
| 5 | MDI2- | | |
| 6 | MDI1- | Receive Data- | Receive Data- |
| 7 | MDI3+ | | |
| 8 | MDI3- | | |

**Table 10 - Gigabit Ethernet RJ-45 Connector Pin-out**

## 6.7. mPCIe A Connector

The PCI Express Mini Card is a small form factor add-in card optimized for mobile computing and embedded platforms. It is not hot-swappable. PCI Express Mini Cards are popular for implementing features such as wireless LAN and communication modules. A small footprint connector on the carrier board provides the ability to insert different removable PCI Express Mini Cards.



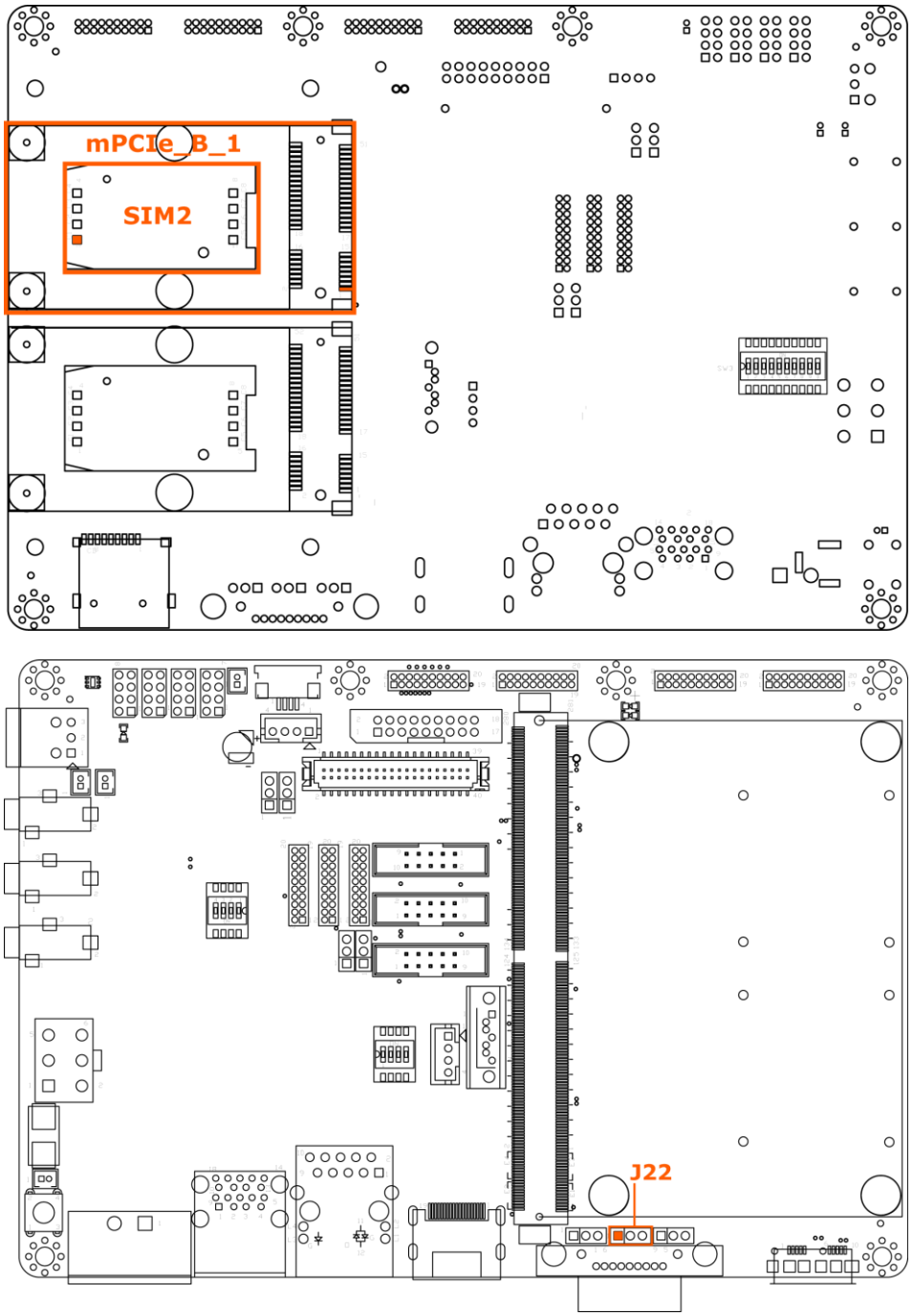




| J21 (mPCIe WAN ON/OFF) | ON (default) | OFF |
|---|---|---|
| 1-2 | ON | OFF |
| 2-3 | OFF | ON |

**Table 11: jumper settings to switch WAN ON/OFF**

## 6.8. mPCIe B Connector

The PCI Express Mini Card is a small form factor add-in card optimized for mobile computing and embedded platforms. It is not hot-swappable. PCI Express Mini Cards are popular for implementing features such as wireless LAN and communication modules. A small footprint connector on the carrier board provides the ability to insert different removable PCI Express Mini Cards.




| J22 (mPCIe WAN ON/OFF) | ON (default) | OFF |
|---|---|---|
| 1-2 | ON | OFF |
| 2-3 | OFF | ON |

**Table 12: jumper settings to switch WAN ON/OFF**

## 6.9. SATA Connector

Serial ATA (SATA) is a serial interface for connecting storage devices (mainly hard disks) and was defined to replace the old parallel ATA interface. Serial ATA uses a point-to-point serial connection between the system and the storage device. The first generation of standard Serial ATA provides a maximum effective data transfer rate of 150MB/s per port. With the second generation SATA II, an effective transfer rate of up to 300MB/s per port is possible. With the third generation SATA III, an effective transfer rate of up to 600MB/s per port is possible.

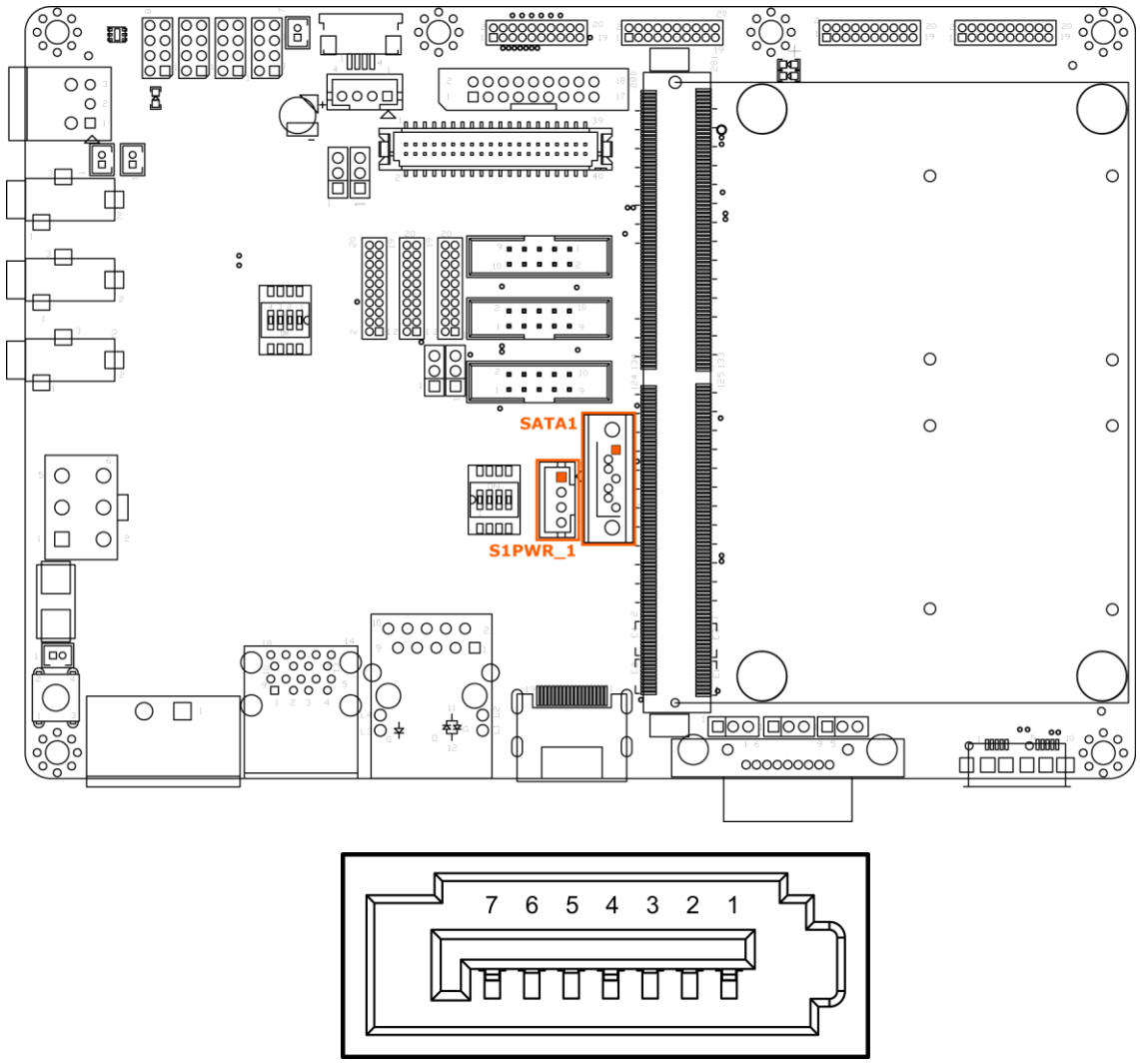



**Figure 26 - Serial ATA Connector**

| Pin # | Signal | Description |
|---|---|---|
| 1 | GND | Ground |
| 2 | TX+ | Transmitter differential pair signal |
| 3 | TX- | |
| 4 | GND | Ground |
| 5 | RX- | Receiver differential pair signal |
| 6 | RX+ | |
| 7 | GND | Ground |

**Table 13 - Serial ATA Connector Pin-out**

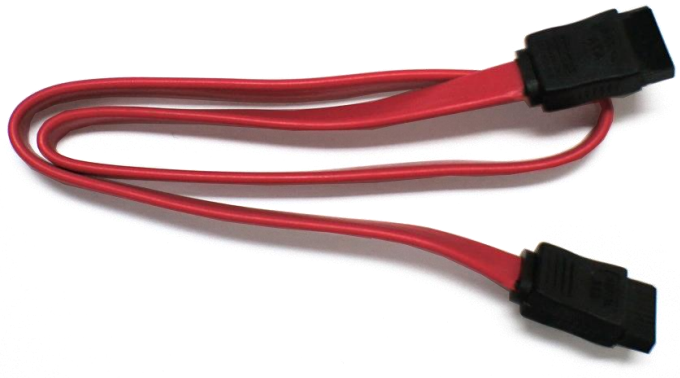
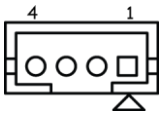


**Figure 27: SATA DATA Cable for the SATA1 connector**




| S1PWR_1 (connector) | |
|---|---|
| 1 | VCC12V |
| 2 | GND |
| 3 | GND |
| 4 | +5V |

**Table 14 - Serial ATA Power Connector Pin-out((wafer 4 pin, 2.0 mm pitch)**

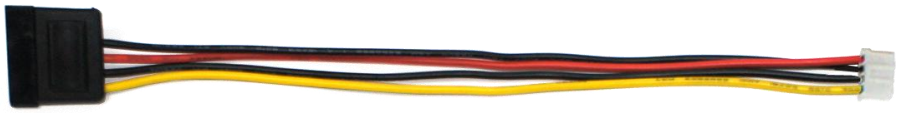


**Figure 28: SATA Power Cable for the S1PWR_1 connector**

| Pin # | Signal | Description |
|---|---|---|
| 1,2,3 | +3.3V | 3.3V Power supply |
| 4,5,6 | GND | Ground |
| 7,8,9 | +5V | 5V Power supply |
| 10,11,12 | GND | Ground |
| 13,14,15 | +12V | 12V Power supply |

**Table 15 - Serial ATA Power Connector Pin-out**

## 6.10. USB

The EDM1 Carrier Board contains 2 USB3.0 USB Hosts connectors which are connected to a USB hub controller.

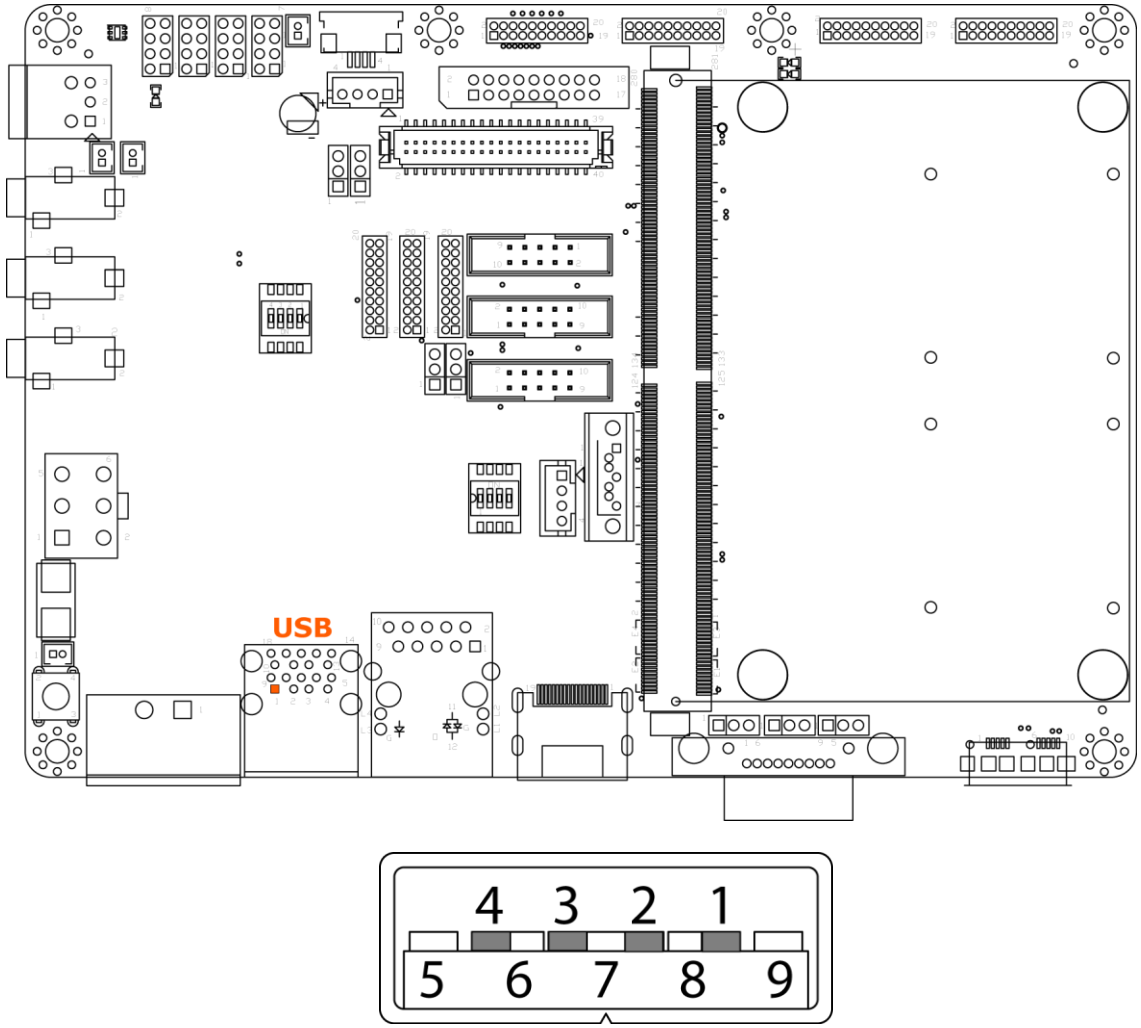


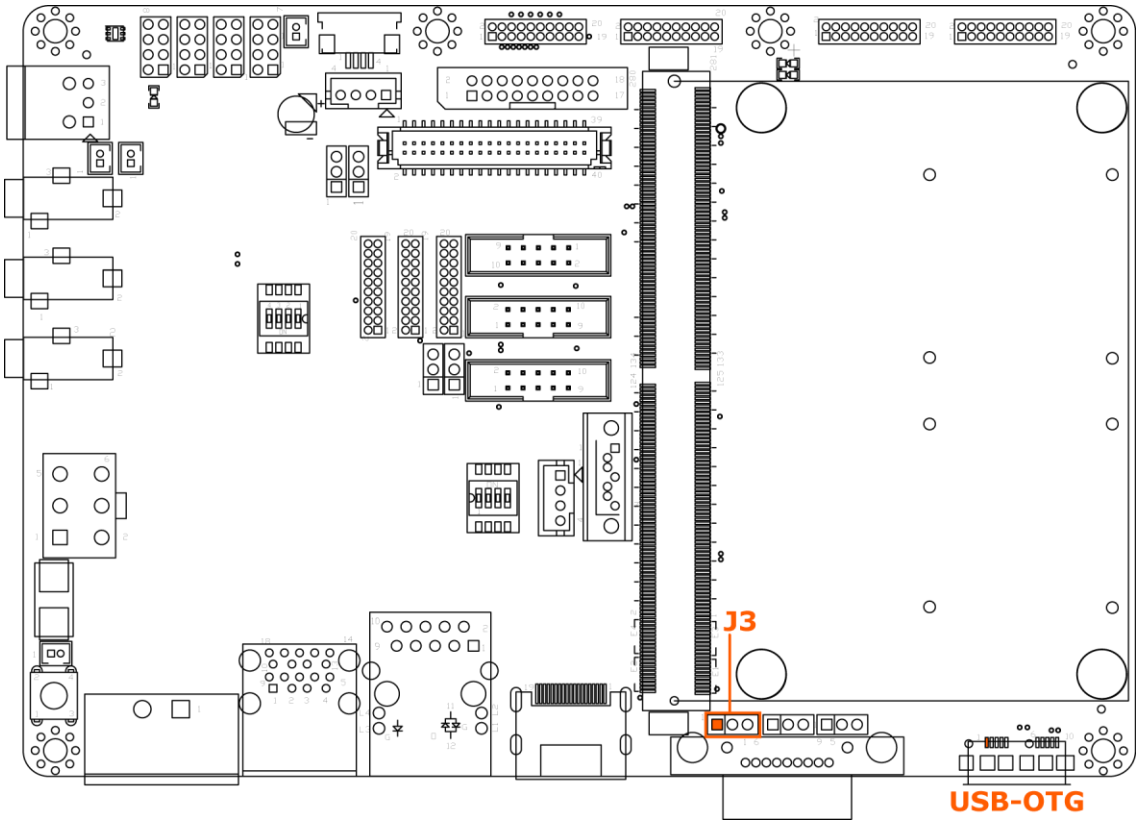

**Figure 29 - USB Host Connector**

| Pin # | Signal | Description |
|---|---|---|
| 1 | VBUS | 5V Uviversal Serial Bus Power |
| 2 | USB_D- | Universal Serial Bus port 2 differential pair signal |
| 3 | USB_D+ | |
| 4 | GND | Ground |
| 5 | StdA_SSRX- | Universal Serial Bus Superspeed receiver differential pair signal |
| 6 | StdA_SSRX+ | |
| 7 | GND | Ground |
| 8 | StdA_SSTX- | Universal Serial Bus Superspeed transmitter differential pair signal |
| 9 | StdA_SSTX+ | |

**Table 16 - USB connector Pin-out**

## 6.11. USB-OTG

The USB-OTG is a connector that can be switched from Client to Host by setting the jumper on pin header J3.




| USB OTG Type | J3 |
|---|---|
| Client/ OTG (Default) | 1-2 |
| Host | 2-3 |

**Table 17: Host / Client setting with jumper J3**

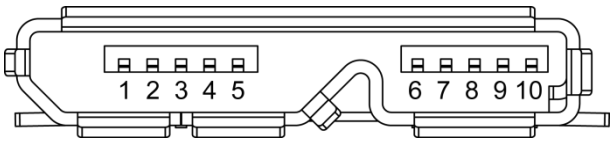


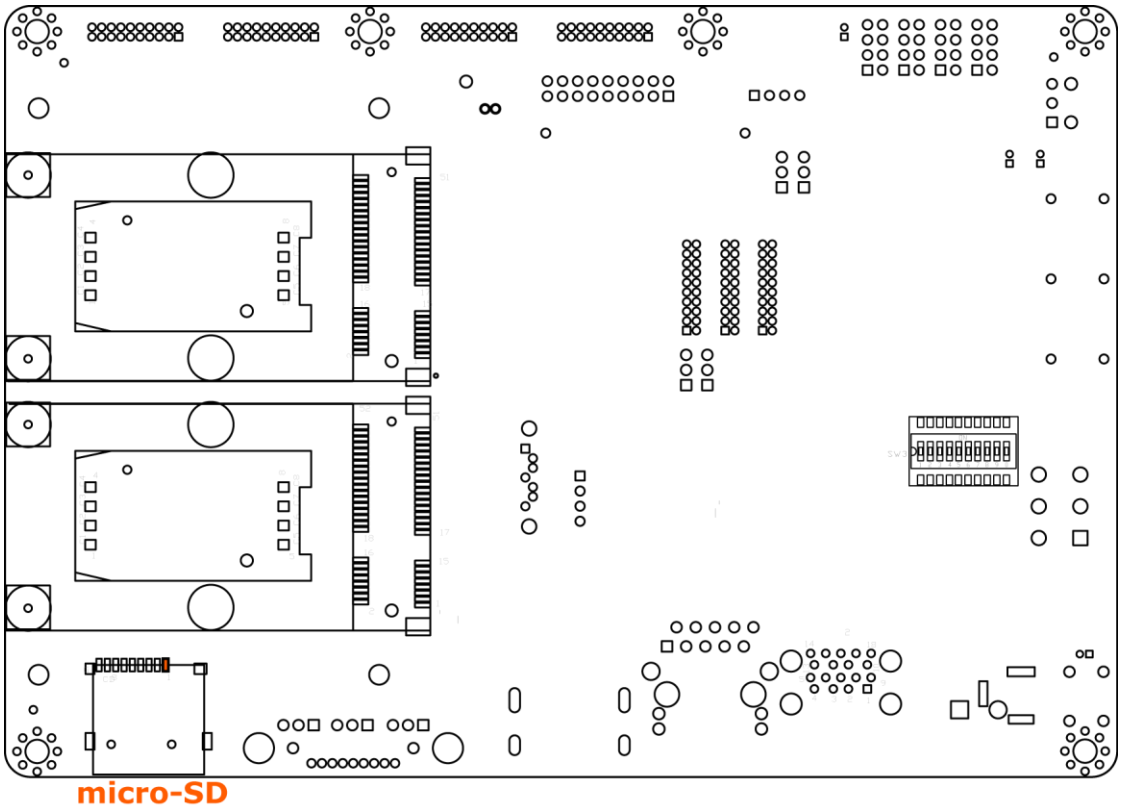

**Figure 30: USB-OTG connector pin out**

| Pin # | Signal | Description |
|---|---|---|
| 1 | VBUS | Ground |
| 2 | USB_D- | Universal Serial Bus port 2 differential pair signal |
| 3 | USB_D+ | |
| 4 | USB_OTG_ID | Universal Serial Bus On-The-Go detection signal |
| 5 | GND | Ground |
| 6 | StdA_SSTX- | Universal Serial Bus Superspeed transmitter differential pair signal |
| 7 | StdA_SSTX+ | |
| 8 | GND | Ground |
| 9 | StdA_SSRX- | Universal Serial Bus Superspeed receiver differential pair signal |
| 10 | StdA_SSRX+ | |

**Table 18: USB-OTG 3.0 Connector pin out**

## 6.12. micro SD-card slot

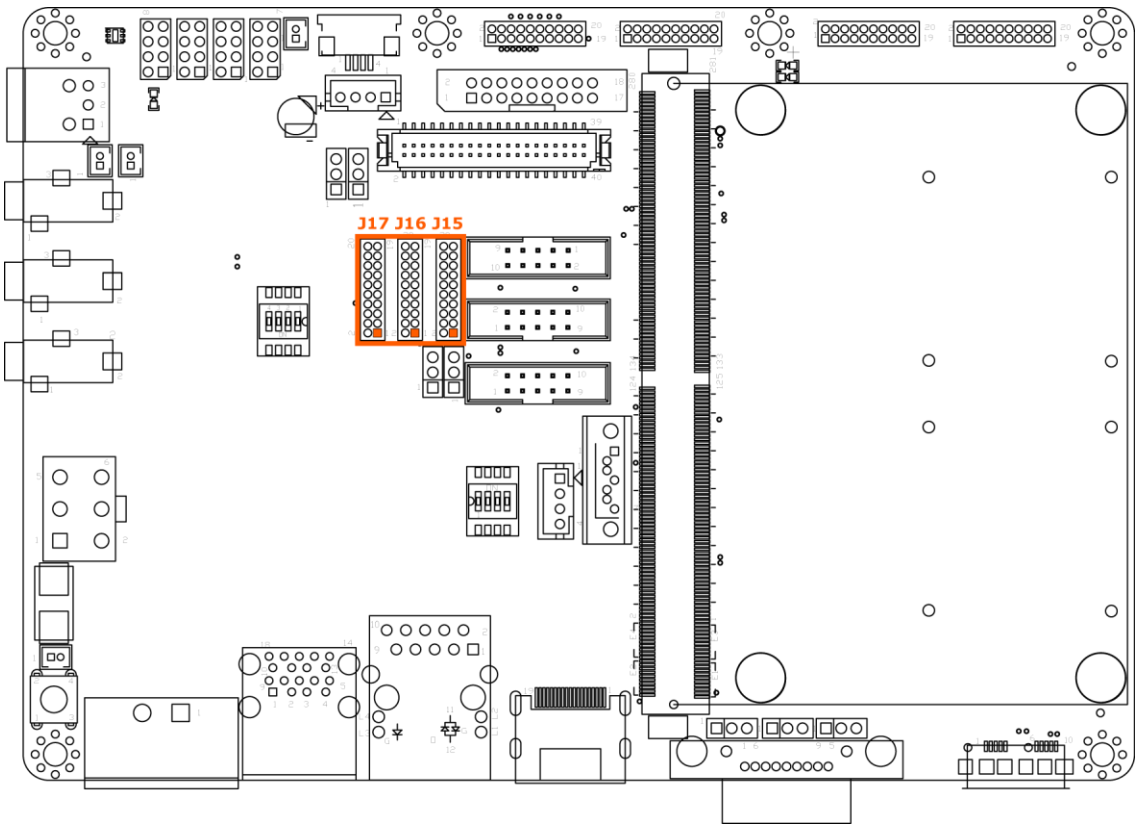
SDIO (Secure Digital I/O) provides an easy to implement solution for high-speed data I/O combined with low power consumption. SDIO cards are fully compatible with SD memory cards. This includes mechanical, electrical, power, signaling and software compatibility. SDIO hosts are able to drive SD cards and MMC (MultiMediaCards) as well as SDIO cards that provide functions such as Ethernet or WLAN, GPS receivers, Bluetooth, modems etc.



## 6.13. GPMC Connectors

Local bus is a common interface in ARM based systems that connect directly, or almost directly, from the CPU to one or more slots on the expansion bus. The significance of direct connection to the CPU is avoiding the bottleneck created by the expansion bus, thus providing fast throughput. There are several local buses built into various types of computers to increase the speed of data transfer. Local buses for expanded memory and video boards are the most common.

The General Purpose Memory Controller (GPMC) can be used to connect to external memory devices such as NOR Flash, NAND Flash, Pseudo SRAM, SRAM or Field programmable Gate Array (FPGA)



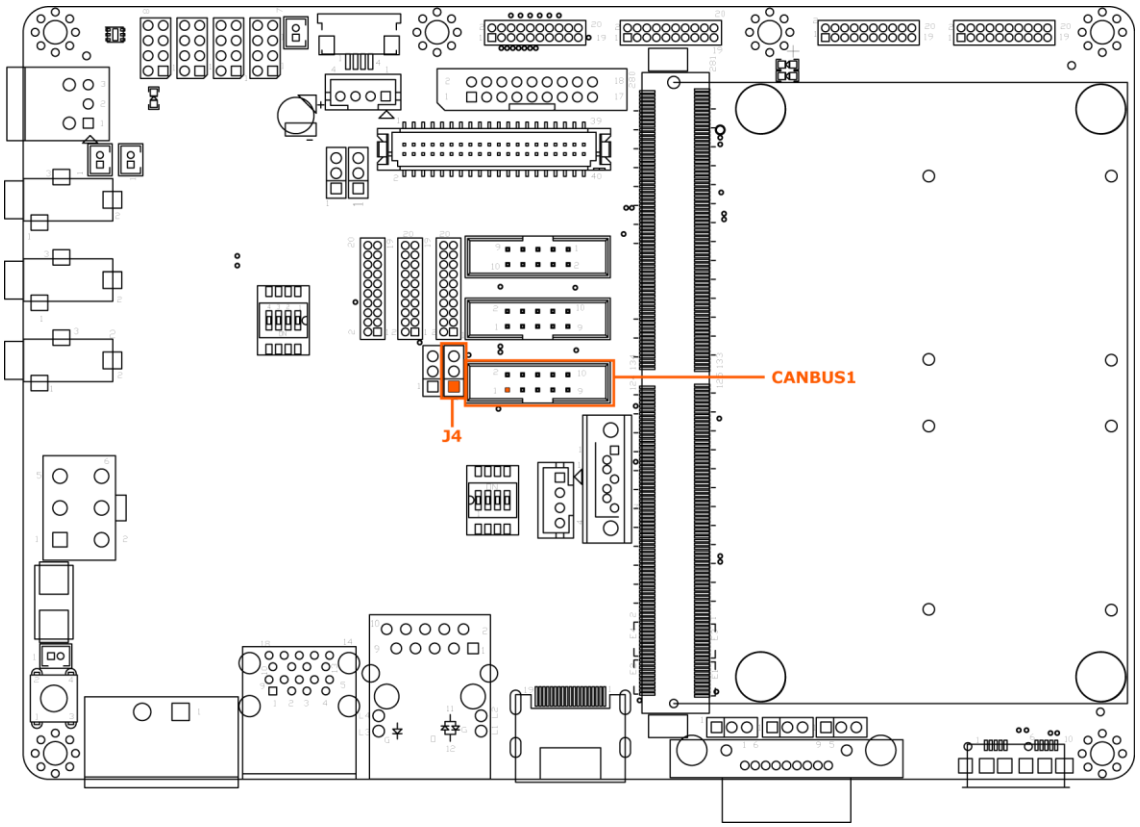

| J15 pin # | Function | J15 pin # | Function |
|---|---|---|---|
| 1 | +3.3V | 2 | GND |
| 3 | GPMC_D0 | 4 | GPMC_D1 |
| 5 | GPMC_D2 | 6 | GPMC_D3 |
| 7 | GPMC_D4 | 8 | GPMC_D5 |
| 9 | GPMC_D6 | 10 | GPMC_D7 |
| 11 | GPMC_D8 | 12 | GPMC_D9 |
| 13 | GPMC_D10 | 14 | GPMC_D11 |
| 15 | GPMC_D12 | 16 | GPMC_D13 |
| 17 | GPMC_D14 | 18 | GPMC_D15 |
| 19 | GPMC_A1 | 20 | GPMC_A2 |

| J16 pin # | Function | J16 pin # | Function |
|---|---|---|---|
| 1 | +3.3V | 2 | GND |
| 3 | GPMC_A3 | 4 | GPMC_A4 |
| 5 | GPMC_A5 | 6 | GPMC_A6 |
| 7 | GPMC_A7 | 8 | GPMC_A8 |
| 9 | GPMC_A9 | 10 | GPMC_A10 |
| 11 | GPMC_WE | 12 | GPMC_RE |
| 13 | GPMC_CLE | 14 | GPMC_ALE |
| 15 | GPMC_WAIT | 16 | GPMC_WP |
| 17 | GPMC_nCSA | 18 | GPMC_nCSB |
| 19 | GPMC_nCSC | 20 | GPMC_nCSD |

| J17 pin # | Function | J17 pin # | Function |
|---|---|---|---|
| 1 | +3.3V | 2 | +5V |
| 3 | +3.3V | 4 | +5V |
| 5 | +3.3V | 6 | +5V |
| 7 | GPMC_nCSE | 8 | X |
| 9 | $I^2S1\_RXD$ | 10 | $I^2S2\_RXD$ |
| 11 | $I^2S1\_TXFS$ | 12 | $I^2S2\_TXFS$ |
| 13 | $I^2S1\_TXD$ | 14 | $I^2S2\_TXD$ |
| 15 | $I^2S1\_TXC$ | 16 | $I^2S2\_TXC$ |
| 17 | $I^2S1\_CLK$ | 18 | $I^2S2\_CLK$ |
| 19 | GND | 20 | GND |

**Table 19 - GPMC Connector Pin-out (female header 10x2  pitch 1.27 mm)**

## 6.14. CAN BUS1




| CAN BUS1 pin # | Function | CAN BUS1 pin # | Function |
|---|---|---|---|
| 1 | Reserved | 2 | CAN1- |
| 3 | GND | 4 | Reserved |
| 5 | CAN_Shield | 6 | GND |
| 7 | CAN1+ | 8 | Reserved |
| 9 | +5V | 10 | X |

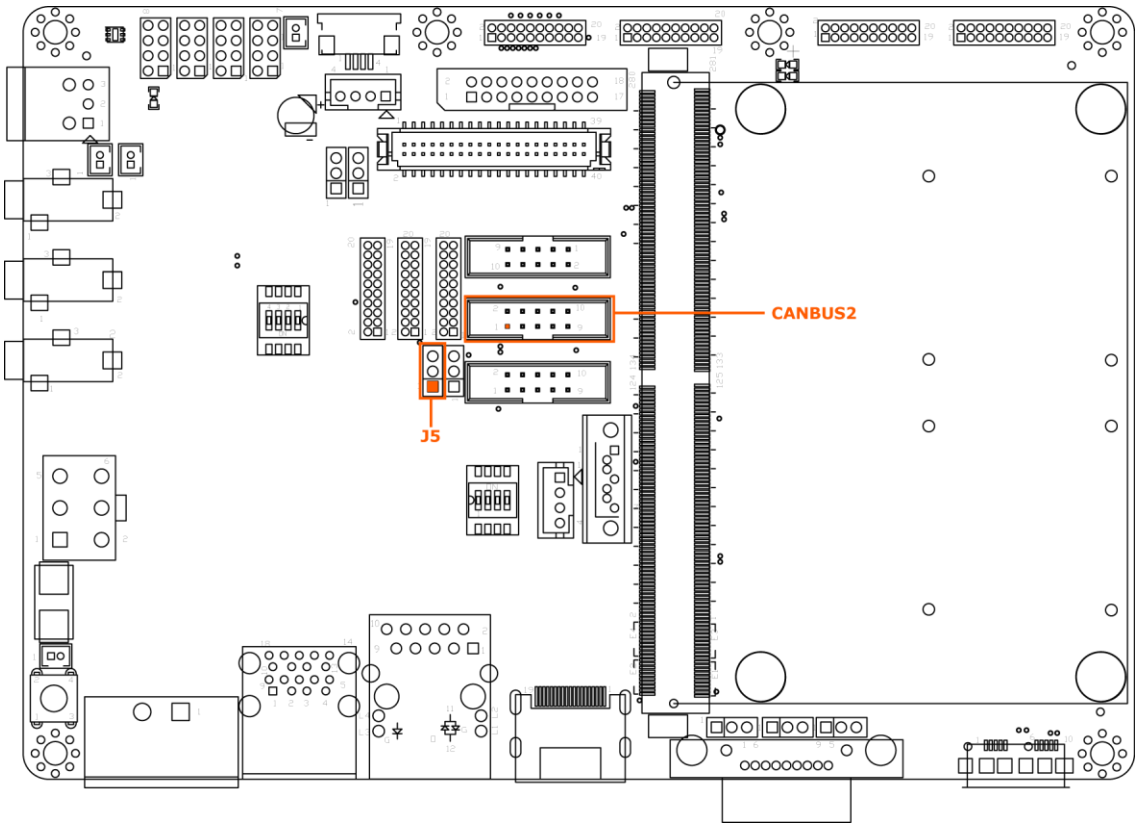
**Table 20: pin out on the CAN BUS1 connector (box header 2x5, 2 mm pitch)**

| CAN BUS1 | J4 |
|---|---|
| Termination | 1-2 |
| Not used | 2-3 |

**Table 21: termination jumper setting for CAN BUS**

**Figure 31: DE9 cable for the CAN BUS1 connector**

## 6.15. CAN BUS2




| CAN BUS2 pin # | Function | CAN BUS2 pin # | Function |
|---|---|---|---|
| 1 | Reserved | 2 | CAN2- |
| 3 | GND | 4 | Reserved |
| 5 | CAN_Shield | 6 | GND |
| 7 | CAN2+ | 8 | Reserved |
| 9 | +5V | 10 | X |

**Table 22: pin out on the CAN BUS2 connector (box header 2x5, 2 mm pitch)**

| CAN BUS2 | J5 |
|---|---|
| Termination | 1-2 |
| Not used | 2-3 |

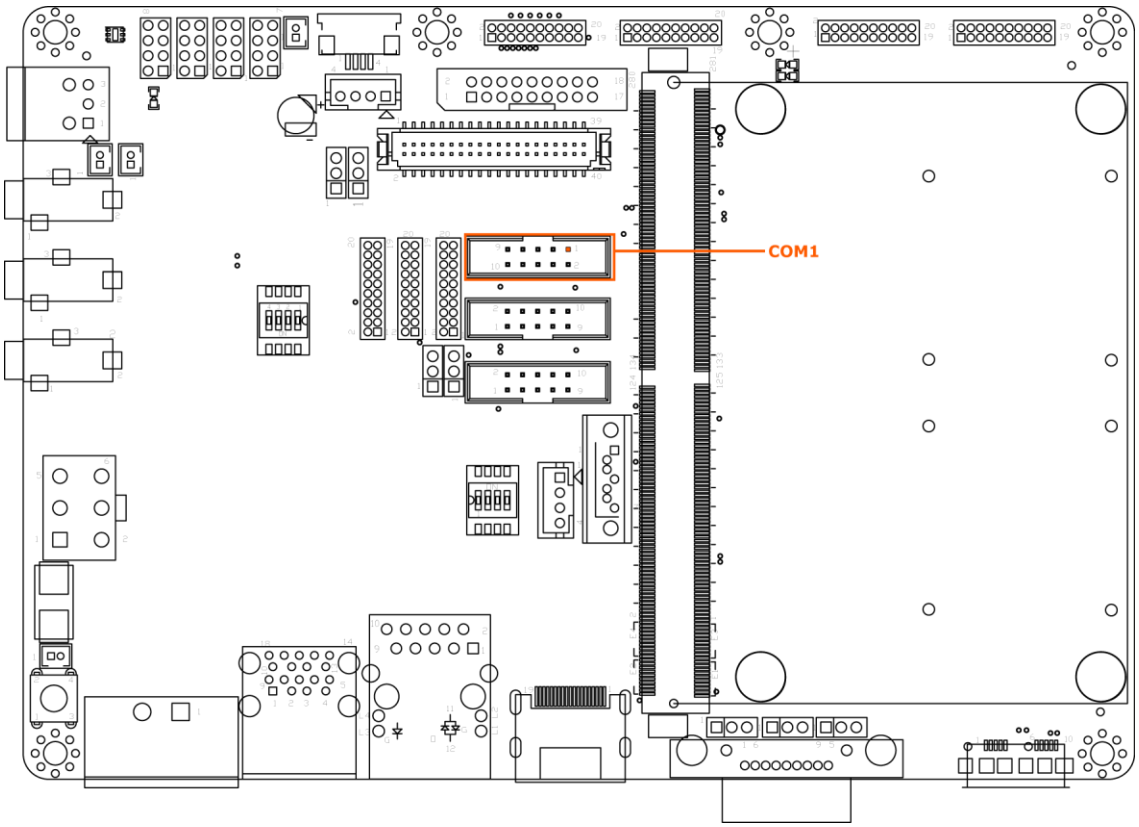
**Table 23: termination jumper setting for CAN BUS**

**Figure 32: DE9 cable for the CAN BUS2 connector**

## 6.16. COM1

A universal asynchronous receiver/transmitter (UART) is a type of "asynchronous receiver/transmitter", a piece of computer hardware that translates data between parallel and serial forms.

The COM1/UART1port can be used to connect a terminal (null modem).




| COM1 pin # | Function | COM1 pin # | Function |
|---|---|---|---|
| 1 | X | 2 | RS232_RX1 |
| 3 | RS232_TX1 | 4 | X |
| 5 | GND | 6 | X |
| 7 | RS232_RTS1 | 8 | RS232_CTS1 |
| 9 | X | 10 | X |

**Table 24: pin out on the COM1 connector (box header 2x5, 2 mm pitch)**

**Figure 33: DE9 cable for the COM1 connector**

## 6.17. COM2

A universal asynchronous receiver/transmitter (UART) is a type of "asynchronous receiver/transmitter", a piece of computer hardware that translates data between parallel and serial forms. UARTs are commonly used in conjunction with communication standards such as EIA RS-232, RS-422 or RS-485.

The COM2 is a DE9 serial port connector. The Serial port can be switched in RS-232, RS-422 or RS-485 modes by setting Dipswitch SW1.

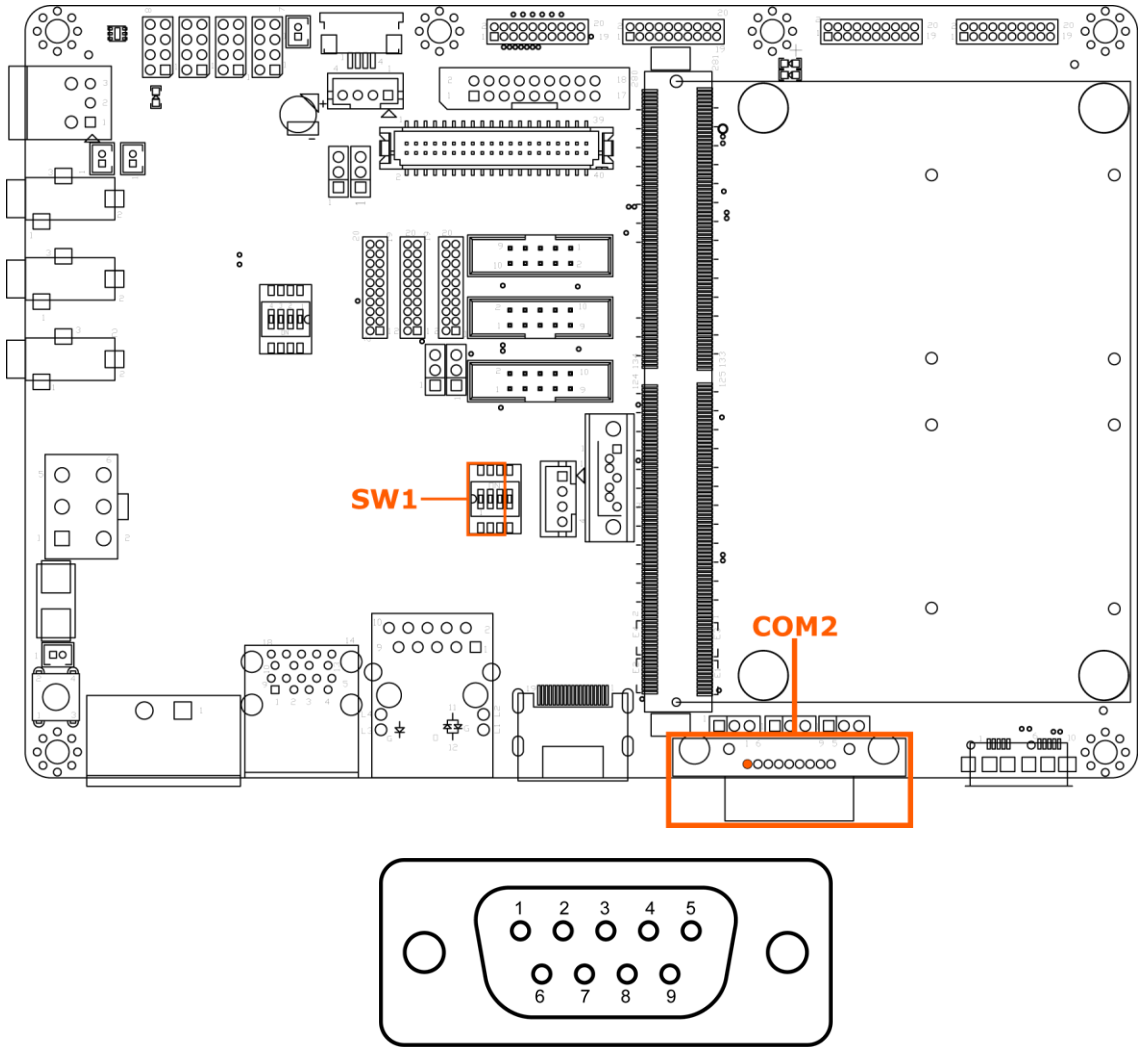
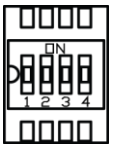



**Figure 34 - DE-9 Serial Port Connector**

| Pin # | RS-232 | RS-422 | RS-485 |
|---|---|---|---|
| 1 | Carrier Detect | TxD- (A) | Data- (A) |
| 2 | Receive Data | TxD+ (B) | Data+ (B) |
| 3 | Transmit Data | RXD+ (B) | |
| 4 | Data Terminal Ready | RxD- (A) | |
| 5 | GND | GND | GND |
| 6 | Data Set Ready | | |
| 7 | Request to Send | | |
| 8 | Clear to Send | | |
| 9 | Ring Indicator | | |

**Table 25 - Serial Port Connector Pin-out**

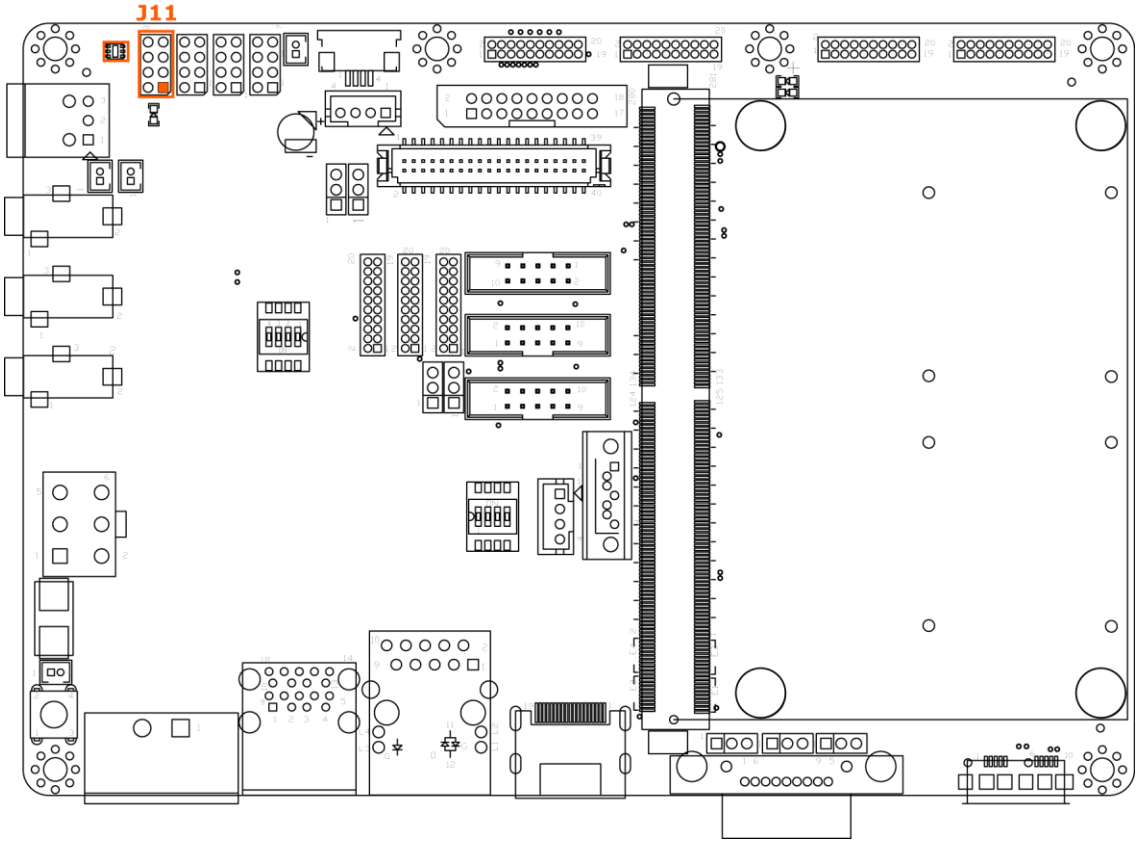



| SW1 (RS-232/485/422 Select on COM2) | RS-422 | RS-485 | RS-232 |
|---|---|---|---|
| 1 | ON | OFF | OFF |
| 2 | OFF | ON | OFF |
| 3 | OFF | OFF | ON |
| **SW1 (Audio output select)** | **SGTL5000** | **TLV320** | |
| 4 | OFF | ON | |

**Table 26: RS-422 / 485 / 232 selection**

## 6.18. Light Sensor

The Intersil ISL29023 is an integrated ambient and infrared light to digital converter with I$^2$C Interface.

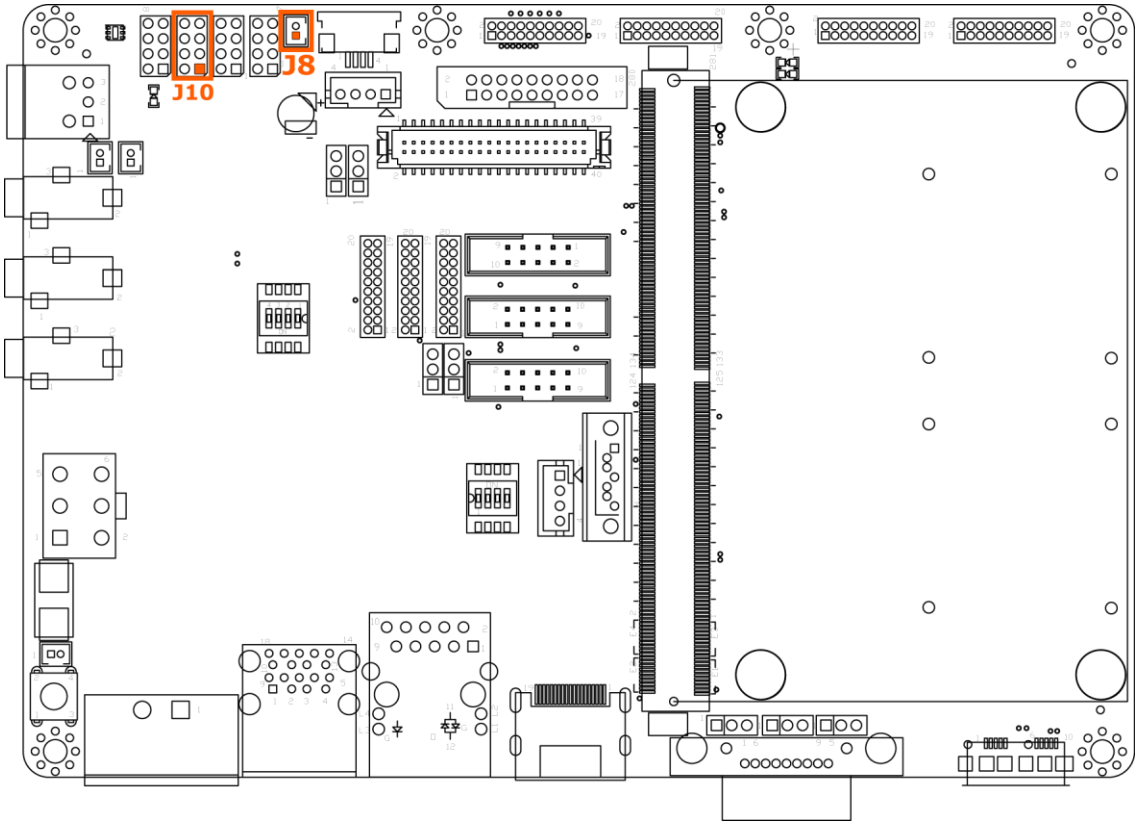



| J11 (I2C Select for Light sensor) | I$^2$C2 | I$^2$C3 (default) |
|---|---|---|
| 1-2 | ON | OFF |
| 3-4 | OFF | ON |
| 5-6 | OFF | ON |
| 7-8 | ON | OFF |

**Table 27: jumper settings for the light sensor I2C selection**

## 6.19. RTC

The power for the RTC is supplied by a CR2032 battery which can be connected to the J8 connector on the carrier board.




| J10 ($I^2C$ Select for RTC) | $I^2C2$ | $I^2C3$ (default) |
|---|---|---|
| 1-2 | ON | OFF |
| 3-4 | OFF | ON |
| 5-6 | OFF | ON |
| 7-8 | ON | OFF |

**Table 28: jumper settings for the RTC I2C selection**

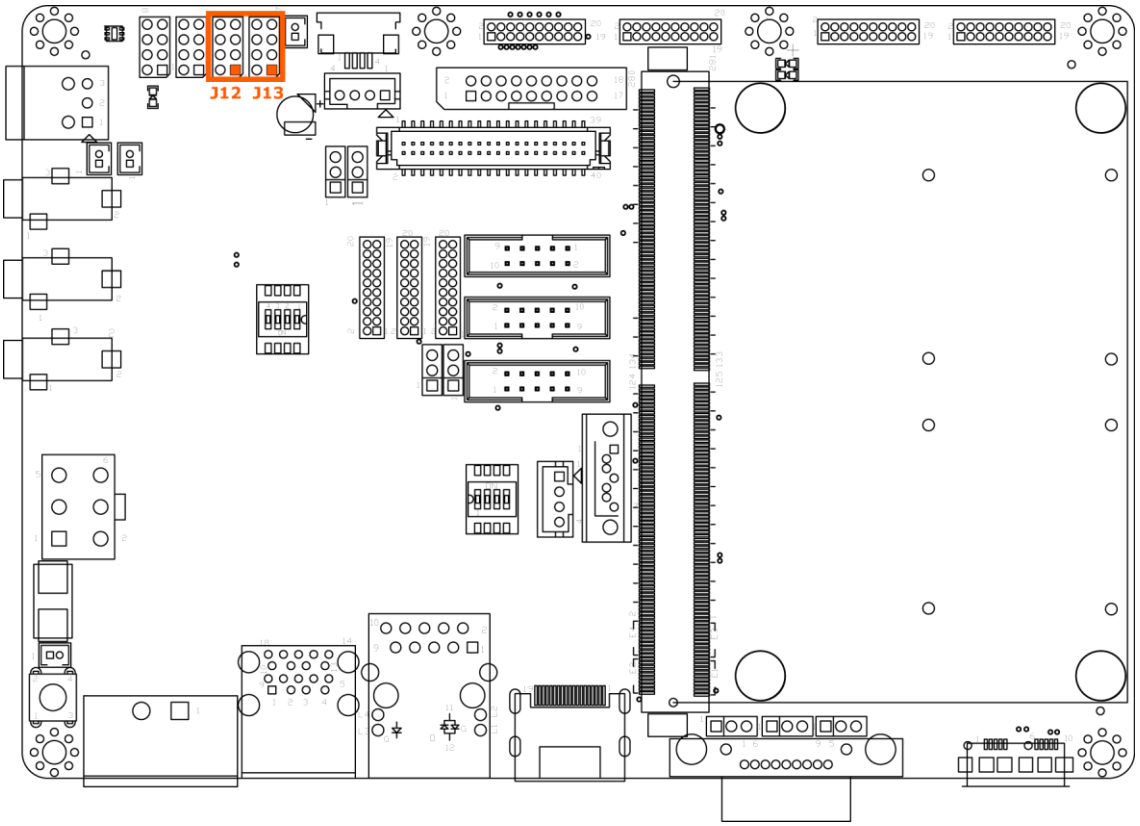
| J8 (RTC) | |
|---|---|
| 1 | Ground |
| 2 | + |

**Table 29 - RTC battery connector Pin-out (wafer 2pin pitch 1.25 mm)**

**Figure 35: CR2032 Battery for RTC**

## 6.20. eCOMPASS and 3 axis Sensors

The Freescale MAG3110 is a small, low-power, digital 3-axis magnetometer. The device can be used in conjunction with a 3-axis accelerometer to realize an orientation independent electronic compass that can provide accurate heading information. It features a standard I2C serial interface output and smart embedded functions. The ST Microelectronics LIS331DLH is the 3 axis linear accelerometer.




| J12 ($I^2C$ Select for eCOMPASS) | $I^2C2$ | $I^2C3$ (default) |
|---|---|---|
| 1-2 | ON | OFF |
| 3-4 | OFF | ON |
| 5-6 | OFF | ON |
| 7-8 | ON | OFF |

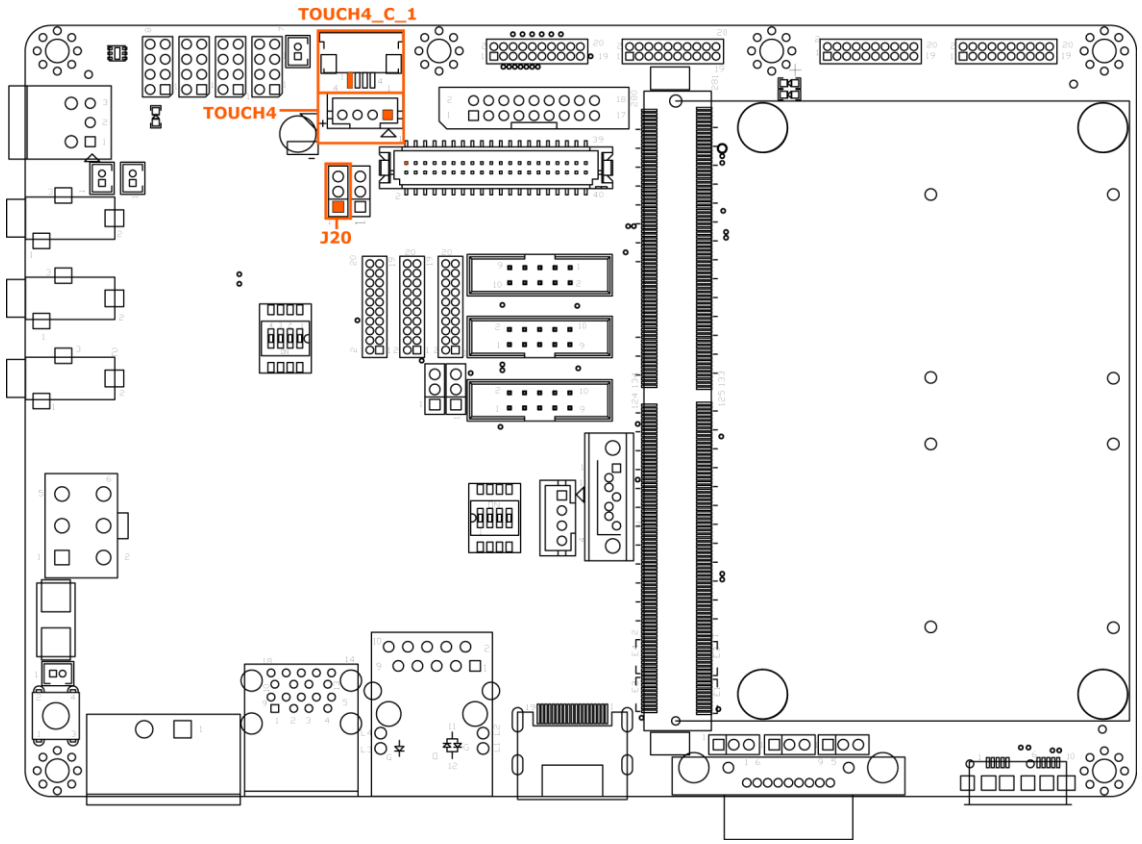
**Table 30: jumper settings for the eCOMPASS sensor I2C selection**

| J13 ($I^2C$ Select for 3 axis sensor) | $I^2C2$ | $I^2C3$ (default) |
|---|---|---|
| 1-2 | ON | OFF |
| 3-4 | OFF | ON |
| 5-6 | OFF | ON |
| 7-8 | ON | OFF |

**Table 31: jumper settings for the 3-axis sensor I2C selection**

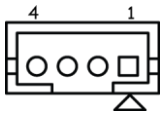
## 6.21. 4-wire touch connectors

The TSC2046 is a 4-wire touch screen controller that is connected to an FPC connector and a wafer connector. The wafer connector can be used to for example connect the optional EDM display kit (TDHJ070NA4RESKIT).




| TOUCH4_C_1 (for FPC) | |
|---|---|
| 1 | XL_ch1 |
| 2 | YD_ch1 |
| 3 | XR_ch1 |
| 4 | YU_ch1 |

**Table 32: FPC connector pin out (4 pins, 1 mm pitch, right angle, upper contact, h=2.5 mm)**




wafer 4 pin 2.0 mm

| TOUCH4 (connector) | |
|---|---|
| 1 | YU_ch1 |
| 2 | XR_ch1 |
| 3 | YD_ch1 |
| 4 | XL_ch1 |

**Table 33: wafer connector pin out ( 4pins, 2 mm pitch)**

| J20 (4 wire Touch ON/OFF) | ON (default) | OFF |
|---|---|---|
| 1-2 | ON | OFF |
| 2-3 | OFF | ON |

**Table 34: Switch ON/OFF touch IC**

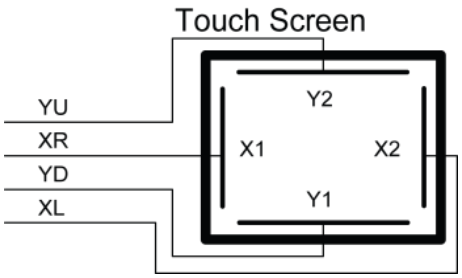



**Figure 36: explanation of touch panel naming**

**Figure 37: optional EDM Display kit (TDHJ070NA4RESKIT))**

## 6.22. 12V DC Power

Connect the 12V DC power adapter with the converter to the Phoenix Combicon MSTB 2.5 connector on the carrier board.

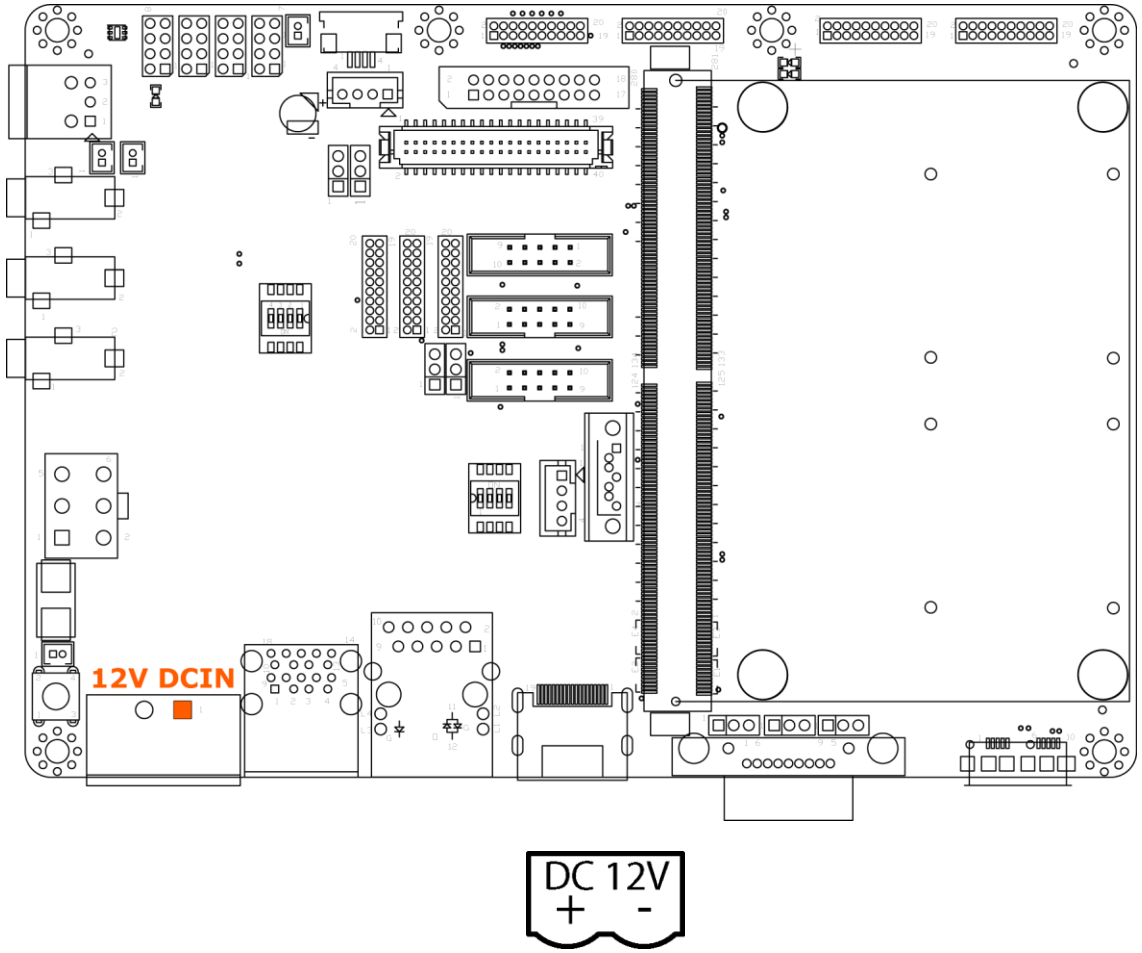
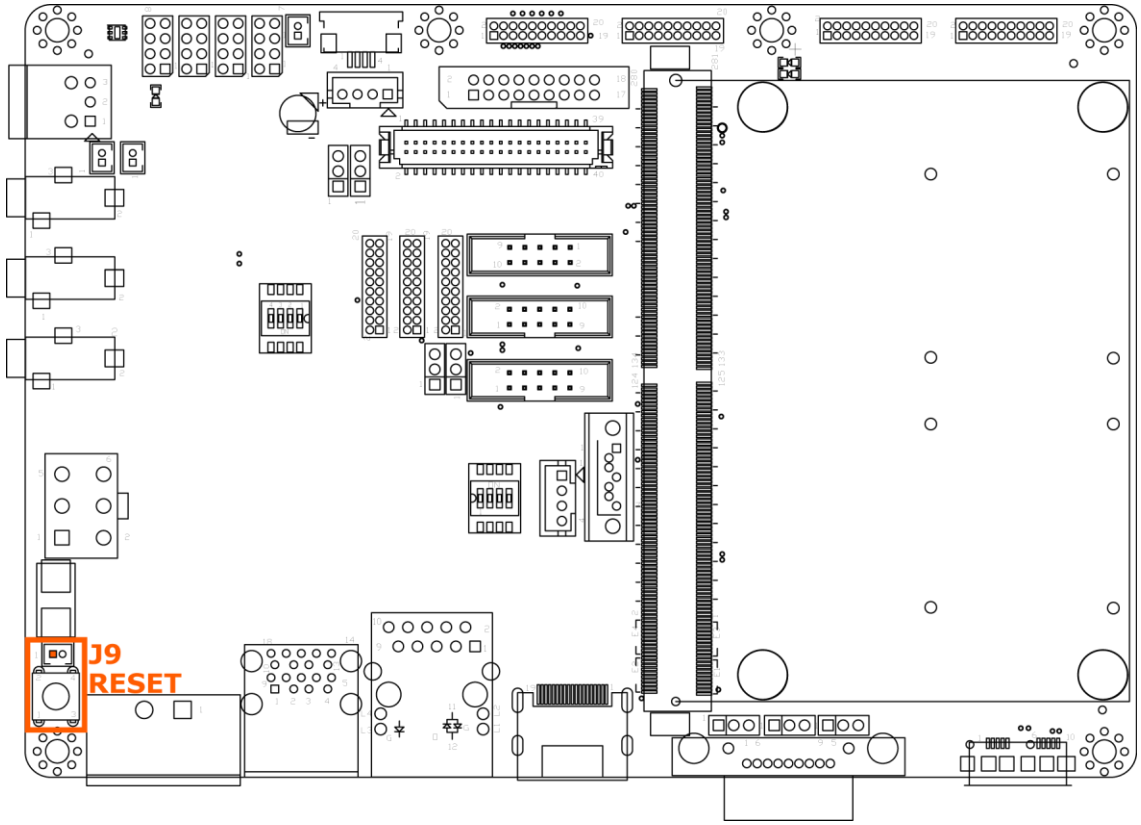



**Figure 38: pin out of the Phoenix Combicon MSTB 2.5 connector**

**Figure 39: converter from power adapter to Phoenix Combicon MSTB 2.5 connector**

## 6.23. Reset button

The hardware reset button is placed next to a small connector. In case the board is mounted in an enclosure, this small connector can be used to connect an external switch.

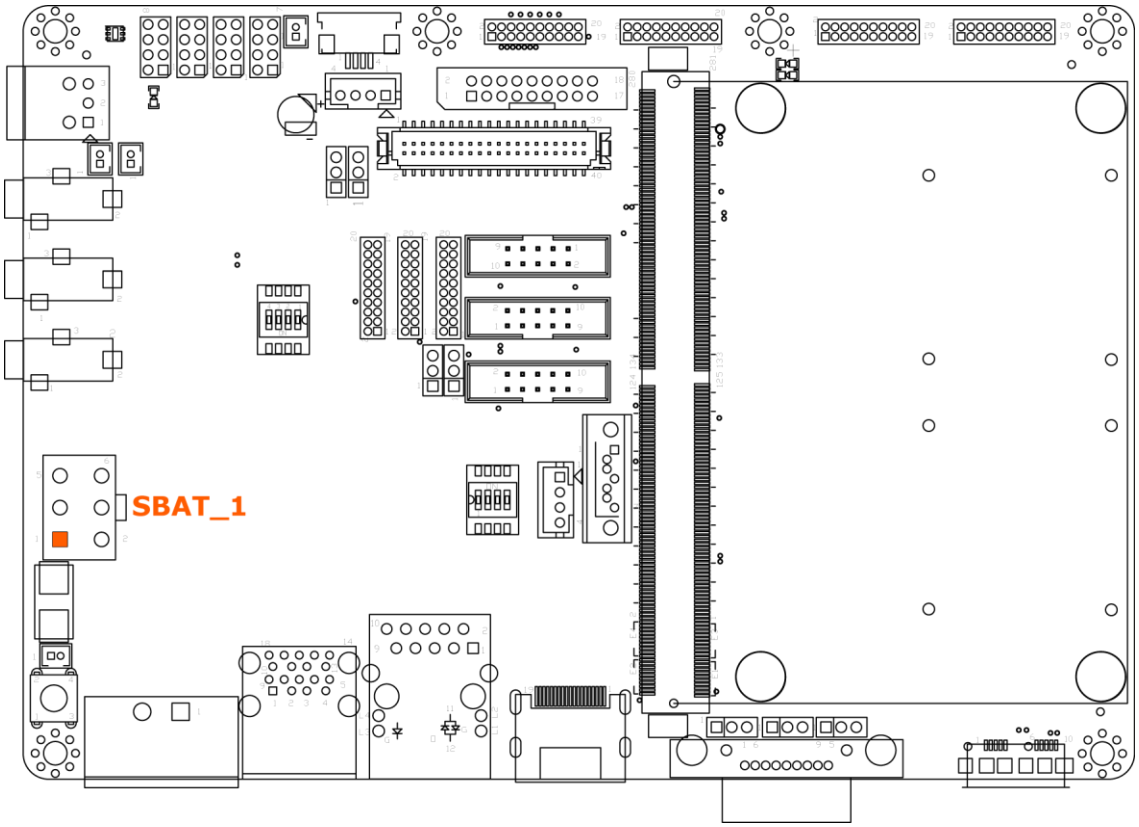



| J9 (reset, ON/OFF) | |
|---|---|
| 1 | Reset |
| 2 | Ground |

**Table 35 - Connector to connect a reset switch externally (wafer 2 pin pitch 1.25 mm)**

## 6.24. Smart Battery

A Smart Battery System (SBS) is used for determining e.g. accurate smart battery capacity readings. It allows operating systems to perform power management operations via a smart battery charger based on remaining estimated run times. Through this communication, the system also controls the amount the battery is charged.

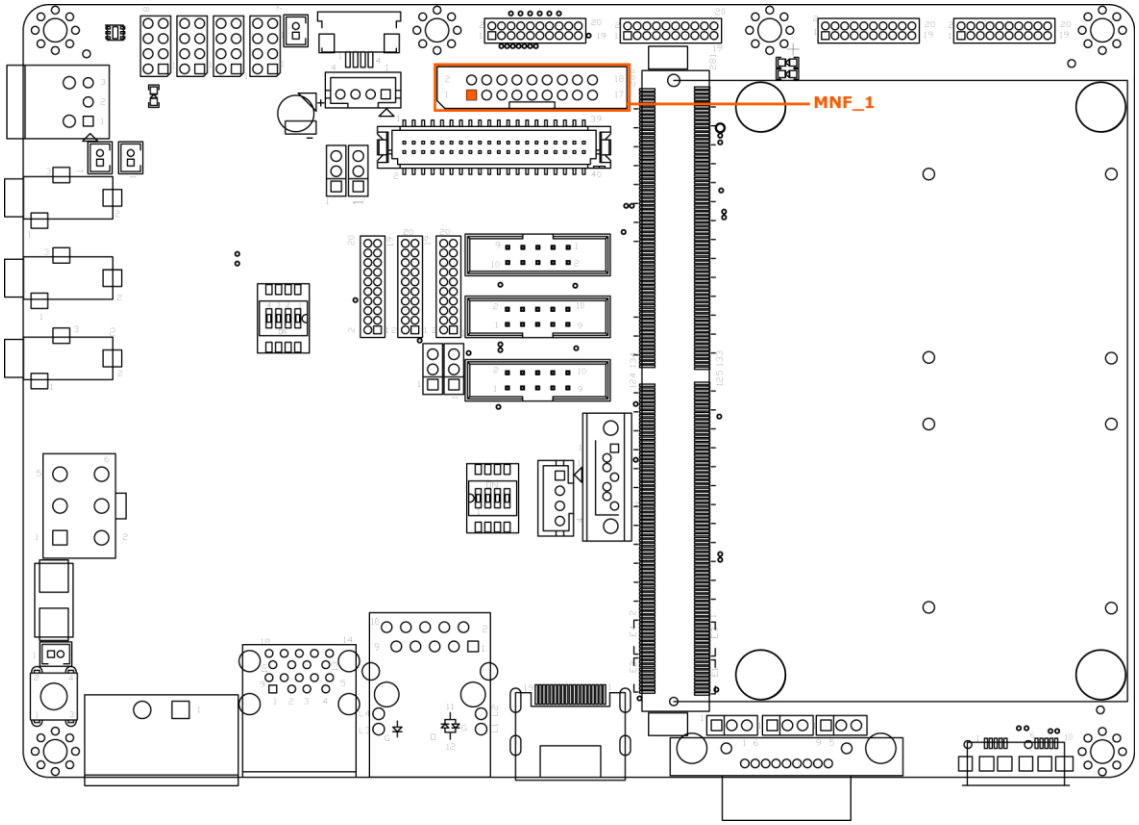



| SBAT_1 Pin # | Function | SBAT_1 Pin # | Function |
|---|---|---|---|
| 1 | GND | 2 | GND |
| 3 | VCC 12V | 4 | VCC 12V |
| 5 | EXT_SCL | 6 | EXT_SDA |

**Table 36 - Smart battery Connector Pin-out (power connector 2x3 pitch 4.2 mm)**

## 6.25. MNF Connector

The MNF connector can for example connect the EDM-MNF-BOOT PCB, which is used to change the boot order to the SD-card.




| MNF pin # | Function | MNF pin # | Function |
|---|---|---|---|
| 1 | RSVD_P267 | 2 | RSVD_P268 |
| 3 | RSVD_P269 | 4 | RSVD_P270 |
| 5 | RSVD_P271 | 6 | RSVD_P272 |
| 7 | RSVD_P273 | 8 | RSVD_P274 |
| 9 | RSVD_P275 | 10 | RSVD_P276 |
| 11 | RSVD_P277 | 12 | RSVD_P278 |
| 13 | Watchdog | 14 | RSVD_P280 |
| 15 | GND | 16 | +3.3V |
| 17 | GND | 18 | +3.3V |

**Table 37 - MNF Connector Pin-out (Box header 9x2 pitch2.0 mm)**

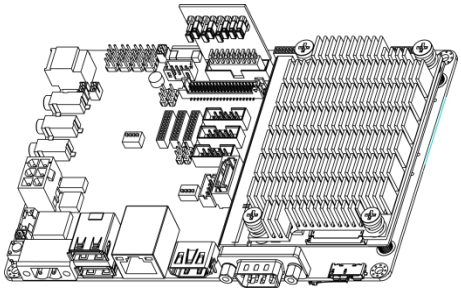


**Figure 40: example of the use of the MNF connector: changing the boot order with the EDM-MNF-BOOT PCB**

# 7. EDM1 Carrier Board dimensions

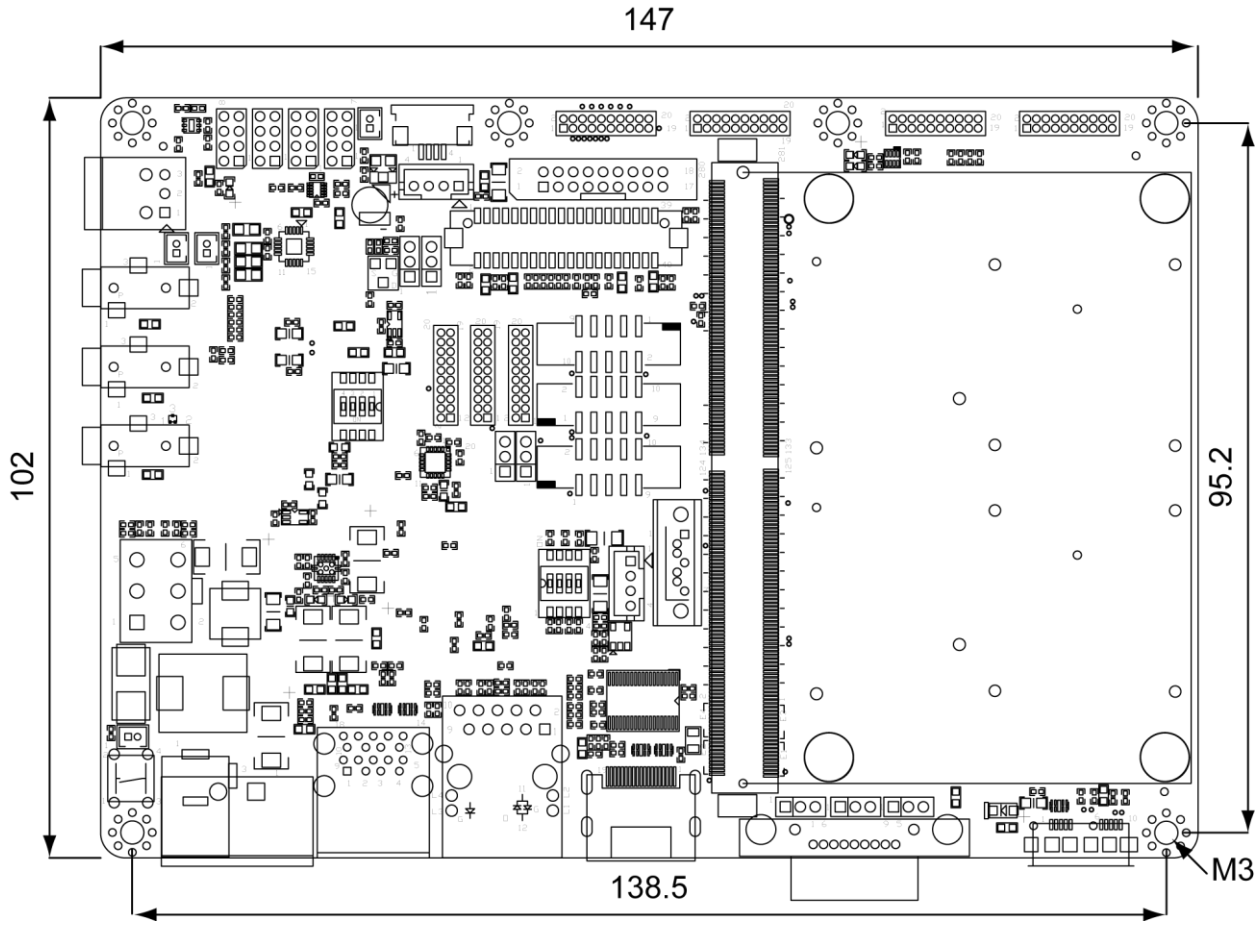



**Figure 41: EDM1 Carrier Board dimensions (Dimensions in mm)**