SoM-9G45M
&
SoM-9M10

User Manual

REV. 2.11

EMAC, inc.
EQUIPMENT MONITOR AND CONTROL
2390 EMAC Way, Carbondale, Illinois 62901
World Wide Web: http://www.emacinc.com
Phone: (618) 529-4525 Fax: (618) 457-0110

Table of Contents

1. Disclaimer

EMAC Inc. does not assume any liability arising out of the application or use of any of its products or designs. Products designed or distributed by EMAC Inc. are not intended for, or authorized to be used in, applications such as life support systems or for any other use in which the failure of the product could potentially result in personal injury, death or property damage.

If EMAC Inc. products are used in any of the aforementioned unintended or unauthorized applications, Purchaser shall indemnify and hold EMAC Inc. and its employees and officers harmless against all claims, costs, damages, expenses, and attorney fees that may directly or indirectly arise out of any claim of personal injury, death or property damage associated with such unintended or unauthorized use, even if it is alleged that EMAC Inc. was negligent in the design or manufacture of the product.

EMAC Inc. reserves the right to make changes to any products with the intent to improve overall quality, without further notification.

2. Introduction

This document describes EMAC's SoM-9G45M & SoM-9M10M System on Modules (SoMs). The SoM-9G45/9M10 is a System on Module, designed to be compatible with EMAC's 200-pin SODIMM form factor. This module is built around the Atmel AT91SAM9G45 & AT91SAM9M10 ARM based microcontrollers, which provide several of its key features. Revision 2.x of this manual references SoM-9G45 / 9M10 PCB Revision 2 or better. See SoM-9G45 / 9M10 Revision 2.0 Product Change Notification for details.

The SoM-9G45/9M10M has an on-board Ethernet PHY, 5 serial ports, a RTC, Micro SD socket, onboard NAND flash, Serial NOR Data Flash, and SDRAM.

In addition to these standard SoM features, the SoM-9G45/9M10M also features a fast 32-bit core, open source software support, and a wide range of controller IO pins.

2.1. Features

- **Small, 200 pin SODIMM form factor (2.66" x 2.375")**
- **Atmel AT91SAM9G45 & AT91SAM9M10 400Mhz ARM based Processor**
- **10/100BaseT Ethernet with on-board PHY**
- **5 Serial ports, 4 with handshake**
- **1 USB 2.0 (High Speed) Host port**
- **1 USB 2.0 (High Speed) OTG Host/Device port**
- **Up to 256 MB of SDRAM**
- **Up to 1 GB of NAND Flash**
- **Up to 8 MB of NOR Serial Data Flash**
- **On-Module Micro SD Card Socket**
- **1 SD/MMC Flash Card Interfaces**
- **Battery backed Real Time Clock**

- **2 SPI and 1 I2C port**
- **2 I2S Audio ports**
- **Timer/Counters and Pulse Width Modulation (PWM) ports**
- **8 Channel 10-bit Analog-to-Digital converter with 4-wire Touchscreen Interface**
- **Image Sensor Interface (ISI), ITU-R BT 601/656**
- **Timer/Counters and Pulse Width Modulation (PWM) ports**
- **8 Channel, 10-bit Analog-to-Digital converter with 4-wire Touchscreen Interface**
- **Graphic LCD Interface with 2D acceleration up to 1280 x 860 Resolution**
- **Multi-format Video Decoder (SoM-9M10 only)**
- **True Random Number Generator**
- **Typical power requirement less than 1 Watt**
- **JTAG for debug, including real-time trace**
- **FREE Eclipse IDE with GCC & GDB development tools**
- **WinCE 6.0 BSP**

3. Hardware

3.1. Specifications

- **CPU:** Embedded Atmel AT91SAM9G45 or AT91SAM9M107 processor running at 400 MHz.
- **Flash:**
  - **SoM-9G45:** 256 MB NAND Flash & 4 MB of Serial Data Flash.
  - **SoM-9M10:** 1 GB NAND Flash & 4 MB of Serial Data Flash.
- **RAM:**
  - **SoM-9G45:** 128 MB 133 MHz DDR2.
  - **SoM-9M10:** 128 MB 133 MHz DDR2 & 128 MB of SDRAM, (256 MB Total).
- **Video:**
  - **SoM-9G45:** LCD Video Interface with up 1280 x 860 resolution.
  - **SoM-9M10:** 2D Accelerated LCD Video Interface with up 1280 x 860 resolution.
    Hardware CODECs: H.264, MPEG-4, MPEG-2, VC-1, H.263.
    Image Processing: Image scaling, color conversion & image rotation.
- **Touchscreen:** 10-Bit 4-wire analog resistive Touchscreen interface.
- **Flash Disk:** 2, 4-bit Parallel or SPI serial SDHC/MMC interfaces one of which terminates to an on-board Micro SD socket.
- **System Reset:** Supervisor with external Reset Button provision.
- **RTC:** Battery backed Real Time Clock/Calendar using 32-bit free running counter.
- **Timers/Counters:** 2, 3 channel, 16-bit timers/counters with capture, compare, and PWM. 20-bit interval timer plus 12-bit interval counter.

- **Watchdog Timer:** External Watchdog/Supervisor using Maxim MAX823 chip.
- **Digital I/O:** 32 General Purpose I/Os with 16 ma. drive when used as an output.
- **Analog I/O:** 8 channel, 10-bit A/D, with 4 channels utilized for 4-wire touchscreen interface.
- **Power:** Power Management Controller allows selectively shutting down on processor I/O functionality and running from a slow clock.
- **JTAG**: JTAG for debug, including real-time trace

Serial Interfaces

- **UARTS:** 5 serial TTL level serial ports, 3 with RTS/CTS handshaking & Auto RS485 (each UART requires external RS level shifting).
- **SPI:** 2 High-Speed SPI ports with Chip Selects.
- **I2C:** 1 multi-mode I2C port.
- **Audio:** 2, I2S Synchronous Serial Controller with analog interface support
- **USB:**
    - 1 USB 2.0 High Speed Host
    - 1 USB 2.0 High Speed Host or Device (USB OTG) software configurable

Ethernet Interface

- **MAC:** Ethernet on chip MAC
- **PHY:** Micrel KSZ8041 with software PHY shutdown control
- **Interface:** IEEE 802.3u 10/100 BaseT Fast Ethernet (requires external magnetics and Jack)

Bus Interface

- Local ARM AT91SAM9G45 / 9M10 Bus accessible through SODIMM provides 22 address lines, 16 data bus lines, and control lines.

Mechanical and Environmental

- **Dimensions:** SODIMM form factor with the length dimension extended (2.66" x 2.375")
- **SODIMM TYPE:** 200 Pin DDR1 (not compatible with DDR2)
- **Power Supply Voltage:** +3.3 Volts DC +/- 5%
- **Power Requirements:** (128MB SoM-9G45)
    - Typical 3.3 Volts @ 260 mA. (less than 1 watt)
    - Max current draw during boot process: 285 mA.
    - Constant busy loop: 270 mA.
    - Constant busy loop with Ethernet PHY disabled : 205 mA.
    - Idle system: 250 mA.
    - Idle system with Ethernet PHY disabled : 175 mA.
    - APM sleep mode using slow clock with Ethernet PHY disabled : 25 mA.
    - APM sleep mode using slow clock with Ethernet PHY enabled : 115 mA.
- **Operating Temperature:** -40 ~ 85° C (-40 ~ 185 ° F), fanless operation
- **Operating Humidity:** 0%~90% relative humidity, non-condensing

3.2. Real Time Clock

The SoM-9G45 / 9M10 emulates a real time clock using the AT91SAM9G45 / 9M10's onboard real time timer. Battery backup is provided from the carrier board using the VSTBY pin. The SoM-9G45 / 9M10 will retain the RTT value register during reset and hence use it as a RTC. The RTC has the provision to set Alarms that can interrupt the processor. For example the processor can be placed in sleep mode and then later awakened via the Alarm function.

3.3. Watchdog Timer

The internal Watchdog Timer provide with the AT91SAM9G45 / 9M10 is not very functional due to the fact that it cannot be reprogrammed. The SoM-9G45 / 9M10 therefore provides an external Watchdog Timer/Supervisor (MAX6747) with an extended watchdog timeout period of 1.42 seconds (±10%). Upon power-up the Watchdog is disabled and does not require pulsing. To start the Watchdog it must first be enabled. This is done by configuring port line PA9 as an output and setting it low in software. Once enabled, the Watchdog should be pulsed, using port line PA8, continually every 1.28 seconds or faster to prevent the Watchdog from timing out and resetting the module. If you are using the watchdog to force a system reset, you may need up to 1.56 seconds of inactivity before the Watchdog reset will occur. The watchdog is automatically disabled upon reset but it can also be disabled by setting PA9 high.

3.4. Status LED

The SoM-9G45 / 9M10 provides a user programmable Green status LED. To control this LED use GPIO port line PA7. Setting the port line high will turn on the LED.

3.5. External Connections

The SoM-9G45/9M10M connects to a carrier board containing its connectors, power supply and any expansion IO, through a standard gold-plated SODIMM 200-pin connection shown below.

The SoM model will fit in any standard 200-pin SODIMM socket. These connections are designed to be compatible with all EMAC 200-pin SoM products. See EMAC SoM 200-pin SODIMM Pinout Specification to see how other 200-pin SoMs pinouts line up with the SoM-9G45/9M10M's pinout.

The use of the DDR SODIMM form-factor for EMAC's SoMs is a sound choice that has been proven rugged and reliable in the laptop and embedded SBC markets.

The remainder of this section describes the pinout as it applies specifically to the SoM-9G45/9M10M processor.

3.5.1. System Control & External Bus

The SoM-9G45/9M10M provides a flexible external bus for connecting peripherals. The CPLD of the SoM-200ES Carrier board connects through a subset of these connections.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
145	GP_CSA	NCS0		General Purpose Chip Select CS0
146	GP_CSB	NCS4	PC10	General Purpose Chip Select CS4
147	GP_CSC	NCS2	PC13	General Purpose Chip Select CS2
148	GP_CSD/Shutdown	SHDN		Processor Shutdown Output
149	WR	NWR0/NWE		Write Signal
150	RD	NRD		Read Signal
151	RST_IN	~RST_IN		Processor Reset
152	RST_OUT	~RST_OUT		Processor Reset
153	WAIT	NWAIT	PC15	Shutdown Control
154	~FLASH WP	~FLASH WP		Data Flash Write Protect
54	WAKEUP	WKUP		Processor Wakeup Input
157	BOOT_OPTION0	BMS		Boot0 Option Select
158	BOOT_OPTION1	Flash Disable		Boot1 Option Select
175 – 193	A0 – A18	A0 – A18		Address Bus
194	A19	A19	PC2	Address Bus line A19
195	A20	A20	PC3	Address Bus line A20
196	A23	A23	PC6	Address Bus line A23
159 – 174	D0 - D15	D0 - D15		Data Bus

3.5.2. USB

The SoM 200-pin specification provides for 2 USB hosts and 1 USB device or OTG port. The AT91SAM9G45 / 9M10 does provide pseudo USB USB OTG port. EMAC has mapped this port to both Host B and Host/Device C. This allows the port to be used as a Full time Host port by connection to Host B or for a full time Device port by connection to Port C. The use of Port C also allows for USB OTG in conjunction with VBUS and ID signals. There is a GPIO line that can be utilized to enable USB power if necessary. This is SoM pin# 125, GPIO[11] and is not required if power will always be on. Remember the USB Data lines are differential pairs and need to be routed as such.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
5	Host_A+	HDPA		Host USB 2.0 Port0 + pin
7	Host_A-	HDMA		Host USB 2.0 Port0 - pin
6	Host_B+	NC		No Connection
8	Host_B-	NC		No Connection
9	Host/Device/OTG_C-	HDMB		OTG USB 2.0 Port1 - pin
11	Host/Device/OTG_C+	HDPB		OTG USB 2.0 Port1 + pin
10	USB_OTG_VBUS	TWCK1/ISI_D11	PB11	OTG VBUS
40	USB_OTG_ID	TWD1/ISI_D10	PB10	OTG ID

3.5.3. JTAG

The SoM specifications allows for access to the JTAG lines for the AT91SAM9G45 / 9M10 processor. These connections will allow the Flash to be programmed in circuit via a program running from the processor and also the capability to debug software.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
139	JTAG_TCK	JTAG_TCK	JTAG clock
140	JTAG_TDI	JTAG_TDI	JTAG serial in
141	JTAG_TDO	JTAG_TDO	JTAG serial out
142	JTAG_TMS	JTAG_TMS	JTAG operation mode
143	JTAG_TRST	~JTAG_TRST	Test Reset Signal
144	JTAG_RTCK	NC	Dynamic clock sync

3.5.4. Ethernet

The SoM-9G45/9M10M provides a Micrel KSZ8041 Ethernet 10/100 PHY IC on board. Carrier designers need only run these lines through the appropriate magnetics layer to have a functional Ethernet connection. Remember the RX and TX lines are differential pairs and need to be routed as such.

The LED/configuration pins' state at reset determines the Ethernet's configuration (10-baseT, 100-baseT, autoconfig) and the function of the LED's. The SoM-200ES pull them all high, which configures the chip for network autoconfig, with LED2 functioning as active low link, and LED3 functioning as active low Activity status (Refer to Carrier schematics).

Note: the KSZ8041 only provides two LEDs. Labeling of the LEDs (1-3) was due to a legacy PHY used on other SoMs.

SODIMM Pin#	SoM Pin Name	LXT972 Pin Name	Description
12	GIG D-	NC	GIG Ethernet D- pin
14	GIG D+	NC	GIG Ethernet D+ pin
13	GIG C-	NC	GIG Ethernet C- pin
15	GIG C+	NC	GIG Ethernet C+ pin
16	Ethernet_Rx-/GIG B-	Etherent_Rx-	Low differential Ethernet receive line
18	Ethernet_Rx+/GIG B+	Ethernet_Rx+	High differential Ethernet receive line
17	Etherent_Tx-/GIG A-	Etherent_Tx-	Low differential Ethernet transmit line
19	Ethernet_Tx+/GIG A+	Ethernet_Tx+	High differential Ethernet transmit line
38	LED_LINK/CFG_2	LED_LINK/CFG_2	Ethernet Link LED/Configuration pin
39	LED_ACT/CFG_3	LED_ACT/CFG_3	Ethernet Activity LED/Configuration pin

3.5.6. I^2C

The SoM-200 specification calls for a two-wire I^2C port. The SoM-9G45/9M10M does not have a native hardware I^2C port but does provide two general purpose lines that can be used in this capacity when "bit-banged". Both Linux and CE provide this functionality.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
29	I2CCLK	TWCK0	PA21	Clock pin
30	I2CDATA	TWD0		Data pin

3.5.7. SPI

The AT91SAM9G45 / 9M10 processor provides two (0 and 1) SPI channels for communicating with peripheral devices. The SPI0 bus is connected internally to the serial flash, which uses SPI0_NPCS0 (SPI0_NPCS0 is not brought out to the card fingers). The first Table below lists the lines for SPI channel #0. The second Table below lists the lines for the SPI channel #1. Note SPI Chip Selects (CS) for both Linux & WinCE do not require a specific SPI CS and can use any GPIO.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
22	SPI_MI	SPI0_MISO	PB0	SPI0 serial data in
23	SPI_MO	SPI0_MOSI	PB1	SPI0 serial data out
24	SPI_SCK	SPI0_CLK	PB2	SPI0 serial clock out
25	SPI_CS0	TCLK1/SCK1	PB29	SPI0 slave select line 0
26	SPI_CS1	SPI1_NPCS1/ADTRG	PB28	SPI0 slave select line 1
27	SPI_CS2	SPI1_NPCS2/IRQ	PB18	SPI0 slave select line 2
28	SPI_CS3	SPI1_NPCS3/FIQ	PB19	SPI0 slave select line 3

SPI0 is allocated to the SoM Pin Specification in the SPI section as the default SPI port. This port should be used to maintain compatibility with past and future modules. As mentioned above the AT91SAM9G45 / 9M10 processor provides two (0 and 1) SPI channels, however, other processors may only offer one. The Table below documents the SPI channel #1, which shares pins in the GPIO pin section.

Note: SPI0 is used to access the Boot Data Flash. Any conflict on SoM pins 22, 23 or 24 can render the SoM unbootable. However, the SPI0 Chip Selects are multi-function pins and are shared with other I/O functions. These lines can be used as GPIOs if required without disturbing the boot process.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
125	GPIO11	SPI1_MISO	PB14	SPI1 serial data in
126	GPIO12	SPI1_MOSI	PB15	SPI1 serial data out
127	GPIO13	SPI1_CLK	PB16	SPI1 serial clock out
128	GPIO14	SPI1_NPCS0/RTS0	PB17	SPI1 slave select line 0
134	GPIO15	ISI_MCK/PCK1	PB31	SPI1 slave select line 1

3.5.8. CAN

The SoM-200 specification provides for a CAN port. The SoM-9G45/9M10M does not have a CAN port. EMAC has therefore applied GPIO lines to these SoM pins.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Pin Description
93	CANTX	TXD0	PB19	COM Transmit
94	CANRX	RXD0	PB18	COM Receive

3.5.9. IRQs

The SoM-200 specification allocates three pins as IRQs. Some processors can use virtually any GPIO pin as an IRQ others use predefined pins. The AT91SAM9G45 / 9M10 has predefined pins (IRQ & FIQ) but can use virtually any GPIO as an interrupt. Since the AT91SAM9G45 / 9M10 can use virtually and GPIO pin as an interrupt source and since the IRQ & FIQ pins are used for other functions EMAC has used the following GPIOs as IRQs:

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	SoM Description
129	IRQA	ISI_PCK	PB28	Interrupt A
130	IRQB	ISI_VSYNC	PB29	Interrupt B
131	IRQC	ISI_HSYNC	PB30	Interrupt C

3.5.10. Oscillators

The SoM-200 specification provides for two general-purpose oscillators. These frequencies can vary slightly between modules depending on how they are generated and some modules may not provide 50% duty cycles. The AT91SAM9G45 / 9M10 uses its internal clock outputs (TIO) to generate these frequencies. The frequencies are programmable via software.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	SoM Description
132	OSC0 (high)	TIOB0/SCK2	PD30	~ 8 MHz
133	OSC1 (low)	TIOB1/PWM1	PD31	~ 200 KHz

3.5.11. SD/Multimedia Card

The AT91SAM9G45 / 9M10 processor provides a dual 4-bit MMC/SD card interface using the MCI lines. The SoM-200ES & 210ES Carrier boards can use a parallel MMC/SD interface if available.

The SoM-200 specification provides for three optional SD/MMC control lines. Since these lines are optional and will not always be used they are not part of the SD/MMC group but are part of the GPIO group. SoM pin#s 122, 123, and 124 can be used as SD_LED, SD_Power, and SD_protect respectively.

MCI1 is allocated to the SoM Pin Specification in the SD/MMC section as the default SD port. This port should be used to maintain compatibility with past and future modules. As mentioned about the AT91SAM9G45 / 9M10 processor provides dual (0 & 1) SD ports, however, other processors may only offer one. The the 2nd (MCI port 0) SD port is allocated to the on-module Micro SD card socket.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
31	SDCLK	MCI1_CK/PCK0	PA31	MCI Clock
32	CMD	MCI1_CDA/SCk3	PA22	MCIA Command
33	DAT0	MCI1_DA0/RTS3	PA23	MCIA D0
34	DAT1	MCI1_DA1/CTS3	PA24	MCIA D1
35	DAT2	MCI1_DA2/PWM3	PA25	MCIA D2
36	DAT3	MCI1_DA3/TIOB2	PA26	MCIA D3
37	Card_Detect	MCI1_DA4	PA27	Card Detect

3.5.12. I2S Audio

The AT91SAM9G45 / 9M10 provides dual I2S audio (0 & 1) ports which is accommodated within the SoM specification. Note that there is no CODEC on the SoM and therefore must be provided on the Carrier. In addition the CODEC will require either SPI or I2C for control.

The Master clock is driven On-Module by a 24.576 oscillator divided by two to produce the 12.288 Master clock. This oscillator is off by default and must be turned on via setting GPIO port line PD4 High. To reduce power the oscillator should be turned off when not required.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
86	AudioA_SCLK	TK0/PWM3	PD0	I2S Serial Clock
87	AudioA_LRCLK/Frame	TF0 & RF0	PD1/PD5	I2S Left / Right Clock
88	AudioA_MCLK			I2S Master Clock
89	AudioA_DIN	TD0	PD2	I2S Data Input
90	AudioA_DOUT	RD0	PD3	I2S Data Output

I2S port 0 is allocated to the SoM Pin Specification in the Audio section as the default I2S port. This port should be used to maintain compatibility with past and future modules. As mentioned about the AT91SAM9G45 / 9M10 processor provides dual (0 and 1) I2S ports, however, other processors may only offer one. The Table below documents the 2nd (port 1) I2S port which shares pins in the GPIO pin section.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
121	GPIO7	TK1/PCK0	PD12	I2S Serial Clock
124	GPIO10	TF1 & RF1	PD14/PD15	I2S Left / Right Clock
134	GPIO15	PCK1/ISI_MCK	PB31	I2S Master Clock
123	GPIO9	TD1	PD10	I2S Data Input
122	GPIO8	RD1	PD11	I2S Data Output

3.5.13. Serial Ports

The SoM-200 pin specification has the provision for 4 serial ports. However, the AT91SAM9G45 / 9M10 provides 5 serial ports. The additional serial port is accommodated through the use of alternate SoM pins. COMB (Debug port) is normally the console port. The AT91SAM9G45 / 9M10 processor does not provide full modem handshaking for COMA as called for in the SoM-200 pin specification, therefore EMAC has utilize processor GPIO lines for this function. The RTS lines for each port can be used to achieve auto RS485 direction control. The actual RTS3 & CTS3 lines from the processor are utilized in the SPI section as these are multi-function lines.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	SoM Description
95	COMA_TXD	TXD1	PB4	COMA transmit/GPIO
96	COMA_RXD	RXD1	PB5	COMA receive/GPIO
97	COMA_CTS	CTS1	PD17	COMA CTS/GPIO
98	COMA_RTS	RTS1	PD16	COMA RTS/GPIO
99	COMA_DTR	AC97TX/TIOA5	PD7	COMA DTR/GPIO
100	COMA_DSR	AC97FS/TIOB5	PD8	COMA DSR /GPIO
101	COMA_RI	AC97FS/TIOB5	PD9	COMA RING/GPIO
102	COMB_TXD	DTXD	PB13	COMB transmit/GPIO
103	COMB_RXD	DRXD	PB12	COMB receive/GPIO
104	COMB_CTS	ISI_D6	PB26	COMB CTS/GPIO
105	COMB_RTS	ISI_D7	PB27	COMB RTS/GPIO
106	COMC_TXD	TXD2	PB6	COMC transmit/GPIO
107	COMC_RXD	RXD2	PB7	COMC receive/GPIO
108	COMC_CTS	CTS2/NCS5	PC11	COMC CTS/GPIO
109	COMC_RTS	RTS2	PC9	COMC RTS/GPIO
110	COMD_TXD	TXD3/ISI_D8	PB8	COMD transmit/GPIO
111	COMD_RXD	RXD3/ISI_D9	PB9	COMD receive/GPIO
112	COMD_CTS	AC97RX	PD6	COMD CTS/GPIO
113	COMD_RTS	LCDPWR/PCK0	PE0	COMD RTS/GPIO

The fifth serial port was mapped to the CAN section pins as the AT91SAM9G45 / 9M10 processor does not provide a CAN controller. The following table shows the mapping of these pins.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Pin Description
93	CANTX	TXD0	PB19	COM Transmit
94	CANRX	RXD0	PB18	COM Receive
25	SPI_CS0	RTS0/SPI1_NPCS0	PB17	COM RTS

Note: the RTS0 is allocated as a standard SPI chip select. Using this line as RTS may reduce forward compatibility.

3.5.14. GPIO

This section provides for the SoM general purpose IO section. All of these pins can be configured to be general-purpose digital ports. They can also be configured to take advantage of several alternate functions of the AT91SAM9G45 / 9M10 processor. Alternate functions include Timer/Counters, 2nd SPI, 2nd I2S and ISI video capture.

Five of these GPIO lines have been delineated for other optional functionality. For compatibility with other SoMs it is a good idea to not utilize these lines as GPIO unless required. Additionally, three signals are marked with '*****' can be used for a second SPI port.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
114	GPIO0	LCDMOD	PE1	GPIO/LCD Backlight On/Off
115	GPIO1	ISI_D0	PB20	GPIO
116	GPIO2	ISI_D1	PB21	GPIO
117	GPIO3	ISI_D2	PB22	GPIO
118	GPIO4	ISI_D3	PB23	GPIO
119	GPIO5	ISI_D4	PB24	GPIO
120	GPIO6	ISI_D5	PB25	GPIO
121	GPIO7	TK1/PCK0	PD12	GPIO/USB_Power_Enable
122	GPIO8	RD1	PD11	GPIO/SD_LED
123	GPIO9	TD1	PD10	GPIO/SD_Power
124	GPIO10	TF1/RF1	PD14/PD15	GPIO/SD_Protect
125	GPIO11	SPI1_MISO	PB14	*GPIO
126	GPIO12	SPI1_MOSI	PB15	*GPIO
127	GPIO13	SPI1_SPCK	PB16	*GPIO
128	GPIO14	SPI1_NPCS0/RTS0	PD17	GPIO
134	GPIO15	ISI_MCK/PCK1	PB31	GPIO

3.5.15. Touchscreen / Analog-to-Digital Convertor (ADC)

The SoM-200 Pin Specification allocates SoM pins that can be utilized as Touchscreen or ADC inputs. Also if a touchscreen is not used, the lines that would normally be used in this capacity can also be used as ADC inputs. The AT91SAM9G45 / 9M10 features an 8 channel, 10-bit ADC. The first four lines are used for a typical resistive 4-wire touchscreen. The AT91SAM9G45 / 9M10 does not support 5 or 8 wire touchscreens. If using GPAD4 – 7 in conjunction with the touchscreen the sample rate is limited.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
45	X+/Xr/ADC0	TSAD0/XP	PD20	X+ or ADC0
46	X-/Xl/ADC1	TSAD1/XM	PD21	X- or ADC1
47	Y+/Yu/ADC2	TSAD2/YP	PD22	Y+ or ADC2
48	Y-/Yd/ADC3	TSAD3/YM	PD23	Y- or ADC3
49	SX+/ADC4	GPAD4/SPI0_CS1/PWM0	PD24	SX+ or ADC4
50	SX-/ADC5	GPAD5/SPI0_CS2/PWM1	PD25	SX- or ADC5
51	SY+/ADC6	GPAD6/PCK0/PWM2	PD26	SY+ or ADC6
52	SY-/ADC7	GPAD7/SPI0_CS3/PCK1	PD27	SY- or ADC7

3.5.16. LCD

The SoM-200 specification has provision for up to 24-bit LCDs (8-bits per RGB color). These lines can also be used to provide analog VGA connectivity for use with a conventional monitor by adding a video DAC to the Carrier. A Brightness PWM is also provided to allow for software control of the LCD's Brightness. SoM pin# 114 can be used to turn the LCD backlight On and Off if desired.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	SoM Description
57	LCD_BLUE0	LCDD23	PE23	LCD BLUE0
58	LCD_BLUE1	LCDD24	PE24	LCD BLUE1
59	LCD_BLUE2	LCDD25	PE25	LCD BLUE2
60	LCD_BLUE3	LCDD26	PE26	LCD BLUE3
61	LCD_BLUE4	LCDD27	PE27	LCD BLUE4
62	LCD_BLUE5	LCDD28	PE28	LCD BLUE5
63	LCD_BLUE6	LCDD29	PE29	LCD BLUE6
64	LCD_BLUE7	LCDD30	PE30	LCD BLUE7
65	LCD_GREEN0	LCDD15	PE15	LCD GREEN0
66	LCD_GREEN1	LCDD16	PE16	LCD GREEN1
67	LCD_GREEN2	LCDD17	PE17	LCD GREEN2
68	LCD_GREEN3	LCDD18	PE18	LCD GREEN3
69	LCD_GREEN4	LCDD19	PE19	LCD GREEN4
70	LCD_GREEN5	LCDD20	PE20	LCD GREEN5
71	LCD_GREEN6	LCDD21	PE21	LCD GREEN6
72	LCD_GREEN7	LCDD22	PE22	LCD GREEN7
73	LCD_RED0	LCDD0	PE7	LCD RED0
74	LCD_RED1	LCDD1	PE8	LCD RED1
75	LCD_RED2	LCDD2	PE9	LCD RED2
76	LCD_RED3	LCDD3	PE10	LCD RED3
77	LCD_RED4	LCDD4	PE11	LCD RED4
78	LCD_RED5	LCDD5	PE12	LCD RED5
79	LCD_RED6	LCDD6	PE13	LCD RED6
80	LCD_RED7	LCDD7	PE14	LCD RED7
81	LCD_HORZ/LP	HSYNC	PE4	Horizontal Sync
82	LCD_VERT/FP/FLM	VSYNC	PE3	Vertical Sync
83	LCD_ENABLE/DE/M	BLANK	PE6	Enable
84	LCD_CLK/SFK/SHFCLK	SPCLK	PE5	LCD Clock
85	BCKLIGHT	BRIGHT/GPIOM7	PE2	Backlight Brightness Control

3.5.17. Image Sensor Interface

The Atmel AT91SAM9G45 / 9M10 processor provides a Image Sensor Interface (ISI). This interface shares lines with other functions of the chip. The 200 pin SoM specification does not provide for this interface however the pins are available on the SoM and can be utilized.

The Image Sensor Interface connects a CMOS-type image sensor to the processor and provides image capture in various formats. It does data conversion, if necessary, before the storage in memory through DMA. The interface can accommodate both 8 and 12 bit sensors.

The ISI supports color CMOS image sensor and grayscale image sensors with a reduced set of functionalities. In grayscale mode, the data stream is stored in memory without any processing and so is not compatible with the LCD controller.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
115	GPIO1	ISI_D0	PB20	Sensor Pixel Data Bit0
116	GPIO2	ISI_D1	PB21	Sensor Pixel Data Bit1
117	GPIO3	ISI_D2	PB22	Sensor Pixel Data Bit2
118	GPIO4	ISI_D3	PB23	Sensor Pixel Data Bit3
119	GPIO5	ISI_D4	PB24	Sensor Pixel Data Bit4
120	GPIO6	ISI_D5	PB25	Sensor Pixel Data Bit5
104	COMB_CTS	ISI_D6	PB26	Sensor Pixel Data Bit6
105	COMB_RTS	ISI_D7	PB27	Sensor Pixel Data Bit7
123	COMD_TXD	ISI_D8	PB8	Sensor Pixel Data Bit8
124	COMD_RXD	ISI_D9	PB9	Sensor Pixel Data Bit9
40	USB_OTG_ID	ISI_D10	PB10	Sensor Pixel Data Bit10
10	USB_OTG_VBUS	ISI_D11	PB11	Sensor Pixel Data Bit11
134	GPIO15	ISI_MCK	PB31	Sensor Master Clock
129	IRQA	ISI_PCK	PB28	Sensor Pixel Clock
130	IRQB	ISI_VSYNC	PB29	Vertical Sync
131	IRQC	ISI_HSYNC	PB30	Horizontal Sync

3.5.18. Boot Options

The SoM specification provides two pins for boot-time configuration. On the SoM-9G45/9M10M, these are BMS and Flash Disable. The Boot Mode Select (BMS) pin allows the SoM-9G45/9M10M to be low-level booted from either its internal ROM (3.3V) or external (carrier resident) NOR flash (GND). The Flash Disable pin should be tied to GND to enable the Serial Data Flash and the NAND Flash or 3.3V to disable.

For normal system Boot, the SoM-9G45 / 9M10 should be configured as follows:

- BOOT_OPTION0 – 3.3V
- BOOT_OPTION1 – GND

The Module can high-level boot from either the Serial Data Flash or the NAND Flash (selected through the low-level bootloader). It is recommended to high-level boot from the Serial Data Flash, as this Flash is more reliable than the NAND Flash. The NAND flash is ideal for the Operating System's File System which can normally mark bad blocks.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
157	BOOT_OPTION0	BMS	Serial Boot Mode Select
158	BOOT_OPTION1		Disable Data & NAND Flash

3.5.19. Serial Data Flash

The Module can high-level boot from either the Serial Data Flash or the NAND Flash (selected through the low-level bootloader). It is recommended to high-level boot from the Serial Data Flash, as this Flash is more reliable than the NAND Flash. The NAND flash is ideal for the Operating System's File System which can normally handle marked bad blocks.

The Serial Data Flash is connected to SPI0 and uses SPI0_NPCS0 to enable it. The Serial Data Flash also has a Write Protect Provision. To Write Protect the Serial Data Flash pull SoM pin# 158 low. SoM pin# 85 is pulled up by a 10K ohm resistor on the module. If this feature is required, it would be implemented on the carrier as a jumper or an I/O line.

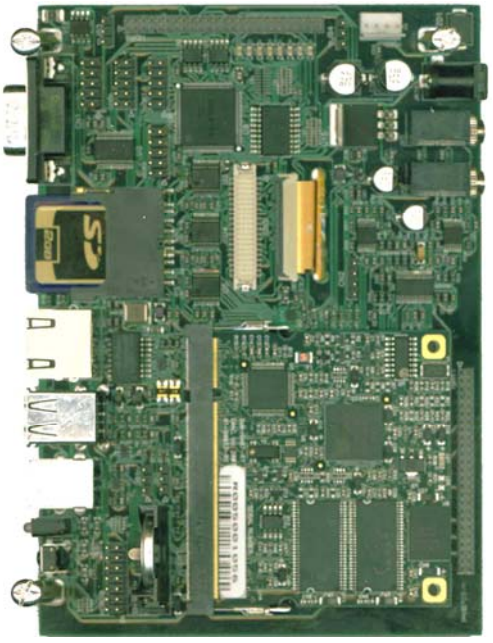
3.5.20. Power Connections

The SoM-9G45/9M10M requires a 3.3V supply for the Bus and I/O voltages. The 1.8V core voltage is regulated on module from the 3.3V. Unlike some other modules no other supply voltage other than 3.3V is required.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
3,4,43,44,135, 136,197,198	3.3VCC	3.3VCC	3.3 Volt SoM Supply Voltage
1,2,20,21,41,42, 91,92,137,138, 155,156,199,200	GND	GND	Digital Ground
53	Analog GND	ADC_GND	Analog Ground
56	VSTBY	Vstandby_3.3	Voltage standby, this is the backup voltage provided to the SoM's RTC. If RTC readings are not important for the application, this can be attached to the 3.3V rail.
55	AV_REF	TSADVREF VDDANA	Analog power/reference. This voltage provides power to the internal analog circuitry of the processor. It can be typically connected to 3.3V. LC filtering for this power signal is provided on-module.

4. Design Considerations

One of the goals of the SoM-9G45/9M10M is to provide a modular, flexible and inexpensive solution capable of delivering high-end microcontroller performance.



4.1. The EMAC SoM Carrier-SoM-200ES

EMAC provides an off the shelf carrier for the SoM-9G45/9M10M module, the SoM-200ES, which provides power to the SoM module as well as wealth of peripheral I/O including audio and LCD. This board comes with full schematics and BOM, and can be used as is, or as a reference for a customer's own design.

http://www.emacinc.com/som/som200ES.htm

NOTE: When designing a carrier be sure to use a 200 pin DDR1 SODIMM socket instead of the more common DDR2 socket. The DDR2 socket is keyed in such a way as to prevent the SoM from being inserted into it. The part number for a compatible DDR1 socket made by Tyco is 1473005-1. This socket will provide 3.0 mm of height from the top of carrier PCB to the bottom of the module PCB. The module specification allows for a 1.5 mm maximum height for bottom components. Therefore this allows the user < 1.5 mm for placing components safely under the module. If more height is need, Tyco as well as other manufacturers make SODIMM sockets with additional height, although these are more expensive.

If using the SoM-9M10's external bus, it is highly recommend to buffer the bus on the carrier board in close proximity to the SoM SODIMM connector (see the SoM-200 carrier schematics for reference).

EMAC also offers a semi-custom engineering service. By modifying an existing design, EMAC can offer quick-turn, low-cost engineering, for your specific application. Additionally, another off-the-shelf SoM 200 pin carrier is available, the SoM-210ES which is used in the PPC-E4.

4.2. Power

The SoM-9G45/9M10M requires a voltage of 3.3V at 300mA for a normal operation, users can get away with using only 3.3V, and simply provide this to all the voltage inputs listed in 3.6. This however, will not provide battery backup for the RTC. Additionally, 5V is required if USB Host capability is required.

4.2.1. Analog Reference

A clean 3.3 Volt source should be provide to this pin if it the A/Ds are required to be accurate. The SoM-9G45/9M10M filters this input before submitting it to the processor. Typically using the 3.3 Volt supply is adequate for Touchscreen use.

4.2.2. Analog Voltage

When designing power for the Analog subsystem there are 4 major considerations, range and accuracy output drive, and rise time.

- **Range**
  The AV_REF pins provide the range. This pin provides power to the analog subsystem, and can take any voltage from 0 to 3.3 Volts. The power supplied to the analog subsystem limits the range of voltages that can be accurately measured. The internal analog converters cannot measure a voltage higher than their power rail. The Analog input range is ~0 to 3.0V when powered by 3.3V. Note if the AV_ACC is powered with less than 3.3V, the full 0 to 3.0V span may not be had.

- **Accuracy**
  The accuracy of the A/D converters is determined by the quality of the voltage applied to the AV_REF pin, which provides the supply/reference voltage to the analog subsystem. The stability of the voltage between this pin and ground will affect the accuracy of the subsystem's measurements. For highly accurate A/D readings it is recommended to use a 3.3V reference on the carrier board.

4.2.3. Battery Backup

The SoM-9G45/9M10M contains 3 potentially non-volatile memory areas, the NAND flash, the real time clock, and the serial flash of the processor. The flash is always non-volatile, the real time clock requires a backup voltage to maintain its data. This backup voltage comes from the VSTBY SoM pin, and should be connected to 3.3 volts.

The RTC will draw approximately 8 uA when the processor is not powered by the 3.3V supply. Be aware that the Static current can rise if the temperature increases to 85° C. When the module is powered no current is drawn from the backup battery supply. If RTC backup is not needed, this can be tied to 3.3V.

The SoM-200ES provides battery backup voltage through a replaceable BR2032, which is a standard 3V 190mA/H 20MM coin battery that can be picked up from most electronics stores.

4.2.4. Shutdown Logic Pins

The SHDN is a digital output only (0 to 3.3V, pulled up on-module), which is driven by the Shutdown Controller on the processor.

The WKUP pin has a Maximum input voltage of 3.3V, but cannot exceed VDDBU.

Both of these pins are connected directly to the processor.

5. Software

The SoM-9G45/9M10M offers a wide variety of software support from both open source and proprietary sources. The hardware core was designed to be software compatible with the Cirrus AT91SAM9G45 / 9M10-EK reference design, which is supported by Linux and WinCE 6.0.

5.1. Eclipse

EMAC provides sample code for the SoM-9G45/9M10M as CDT projects within the free Eclipse IDE. Eclipse is a powerful open-source Java based IDE. It has plug-ins for development and debugging in Java and C, as well as several other languages.

http://www.eclipse.org/

EMAC offers a free download of Eclipse pre-integrated with the CDT plug-in and plug-ins for remote debugging and SVN. Eclipse requires the Java Runtime Environment to be installed on the development system. Currently EMAC only supports the use of Eclipse under the Linux environment for the SoM-9G45/9M10M. The Eclipse environment and JRE for Linux are available online along with user manuals.

ftp://ftp.emacinc.com/PCSBC/Development_Kits/EMAC_Open_Tools/

5.1.1. Eclipse CDT plug-in

The Eclipse CDT plug-in provides a powerful graphical IDE for C development. This plug-in relies on GNU Make to build its files, so its projects are highly portable to other IDE's (or lack of them completely). It also offers a MI based debugger, for plugging into newer gdbs.

http://www.eclipse.org/cdt/

5.2. Das U-Boot Bootloader

The SoM-9G45/9M10M is distributed with Das U-Boot installed. U-Boot is an open source/cross-architecture platform independent bootloader. It supports reading and writing to the flash, auto-booting, environmental variables, and tftp. Das U-boot can be used to upload and run and/or reflash the OS on the SoM-9G45/9M10M without the use of a JTAG cable, or to run stand-alone programs without an OS. SoM-9G45/9M10M modules are shipped with a valid MAC address installed in flash in the protected ethaddr environmental variable of U-Boot. At boot time U-Boot automatically stores this address in a register within the MAC, which effectively provides it to any OS loaded after that point.

5.3. Embedded Linux

EMAC Open Embedded Linux is an open source Linux distribution for use in embedded systems. The current SoM-9G45/9M10M build uses a Linux 2.6 kernel that has been has been patched to support the SoM-9G45/9M10M and SoM-200ES devices.

The distribution contains everything a user could expect from a standard Linux kernel, powerful networking features, advanced file system support, security, debugging utilities, and countless other features.

The SoM-9G45/9M10M will work out of the box with EMAC's Embedded Linux distribution, and EMAC provides the most up to date distribution via FTPSVN. The SoM-9G45/9M10M comes preinstalled with a 2.6.30 or later Linux kernel.

The Bootloader / Linux Console Port defaults to:

- COMB
- 115200 Baud
- N-8-1
- No Handshaking

5.3.1. Linux with Xenomai Real Time Extensions

Xenomai provides real time extensions to the kernel and can be used to schedule tasks with hard deadlines and μs latencies. The Xenomai build is an additional module that can be added to the standard Linux kernel and is available for a one-time inexpensive support/installation fee.

http://www.xenomai.org/

5.3.2. Linux Modules

EMAC provides support for many Linux modules such as: Lighttpd Web Server, PHP, SQLite, Perl, SNMP, DHCP Server, etc. Also, other modules can be added to the standard Linux filesystem and are available for an inexpensive one-time support/installation fee.

5.3.3. Linux 2.6 Public Repository

EMAC Linux 4.0 Distribution integrates a number of kernel patches and device drivers from the open source community along with support for EMAC engineered products. Currently, the kernel for the SoM-9G45M/9M10 is available via our public SVN repository.

https://svn.emacinc.com/public/linux-2.6.30-at91/trunk/

Along with kernel source, EMAC provides the binaries for the kernel and root file system.

ftp://ftp.emacinc.com/Controllers/SoM/SoM-9G45/9M10M/Software/Linux/

5.4. Open Embedded

The Linux build for the SoM-9G45/9M10M is based on the Open Embedded (www.openembedded.org) Linux build system. The current kernel is Linux 2.6.30 or higher patched to support the SoM-9G45/9M10M. Open Embedded is a superior Linux distribution for embedded systems. Custom Linux builds are also available on request.

The basic root filesystem includes:

- Busybox 1.13 or higher
- Hotplugging support
- APM utilities for power management
- Open BSD SSH server
- Telnet/FTP support running under inetd
- busybox-httpd HTTP server
- JFFS2 filesystem with utilities

5.5. ARM EABI Cross Compiler

The popular open source gcc compiler has a stable build for the ARM family. The Embedded Linux kernel and EMAC Eclipse CDT projects use this compiler for building ARM stand alone, and OS specific binaries. The EMAC Eclipse SDK provides source level debugging over either the JTAG port or over Ethernet or serial using gdbserver. The Linux binaries for the ARM EABI cross compiler are available online along with the SDK for the SoM-9G45/9M10M at the following location.

ftp://ftp.emacinc.com/Controllers/SoM/SoM-9G45/9M10M/Tools/

5.6. Windows CE 6.0

In addition to the open source community, a WinCE 6.0 BSP for the SoM-9G45/9M10M is under development and will be available soon.

The Bootloader / WinCE Console/Debug Port defaults to:

- COMB
- 115200 Baud
- N-8-1
- No Handshaking

Note: All of the links in this document are subject to change. Please contact EMAC for updated link locations if necessary.

