SoM-9G25M

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For use with PCB Rev 1 and greater

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1 Introduction

1.1 Features

- Small, 144 pin SODIMM form factor (2.66” x 1.5”)
- Atmel ARM926 Thumb AT91SAM9G25 400Mhz Processor
- 10/100Base T Ethernet with on-board PHY
- 7 Serial ports, 2 with handshake
- 1 USB 2.0 (Full Speed) Host port
- 1 USB 2.0 (High Speed) Host port
- 1 USB 2.0 (High Speed) Device/Host port
- Up to 128 MB of DDR2 RAM
- Up to 64 MB of Serial Flash
- Battery backed Real Time Clock
- SD/MMC Flash Card Interface
- 2 SPI Ports
- 2 I2C Ports
- 1 I2S Audio Port
- 18 GPIO Lines
- 4 Timer/Counters and 4 Pulse Width Modulation (PWM) ports
- 4 Channel 10-bit Analog-to-Digital converter
- Typical power requirement less than 1 Watt
- JTAG for debug, including real-time trace

2 Hardware

2.1 Specifications

- **CPU:** Embedded Atmel AT91SAM9G25 processor running at 400 MHz
- **Flash:** Standard NAND Flash (512MB optional) and 32MB (64MB optional) of Serial Data Flash
- **RAM:** Up to 128MB 133 MHz DDR2 RAM
- **Flash Disk:** 4-bit Parallel or SPI serial SDHC/MMC interface

- **System Reset:** Supervisor with external Reset Button provision
- **RTC:** Real Time Clock/Calendar with battery backed provision using 32-bit free running counter
- **Timer/Counters:** 2, 3 channel, 32-bit timers/counters with capture, compare, and PWM. 20-bit interval timer plus 12-bit interval counter
- **Watchdog Timer:** Processor based watchdog timer
- **Digital I/O:** 32 General Purpose I/Os with 16mA drive when used as an output
- **Analog I/O:** 4 channel 10-bit Analog-to-Digital converter (ADC)
- **Power:** Power Management Controller allows selectively shutting down on processor I/O functionality and running from a slow clock
- **JTAG:** JTAG for debug, including real-time trace
- **Clocks:** PLL synthesized 8M, 200k, 14.3M clock outputs

Serial Interfaces

- **UARTS:** 6 serial TTL level serial ports with Auto RS485 and some with handshaking (each UART requires external RS level shifting)
- **SPI:** 2 High-Speed SPI ports with Chip Selects
- **Audio:** I2S Synchronous Serial Controller with analog interface support
- **USB:** 1x USB 2.0 High Speed Host Port, 1x USB 2.0 Full Speed Host Port, 1x USB 2.0 High Speed Device Port

Ethernet Interface

- **MAC:** AT91SAM9G25 on chip Single MAC
- **PHY:** Single Micrel KSZ8041 PHY with software PHY shutdown control.
- **Interface:** IEEE 802.3u 10/100 BaseT Fast Ethernet (requires external magnetics and Jack)

Bus Interface:

- Local ARM AT91SAM9G25 Bus accessible through SODIMM provides 22 address lines, 16 data bus lines, and control lines

Mechanical and Environmental

- **Dimensions:** SODIMM form factor with the length dimension extended (2.66” x 1.5”)
- **Power Supply Voltage:** +3.3 Volts DC +/- 5%

- **Power Requirements:**
  - Typical 3.3 Volts @ TBD
  - Max current draw during boot process: TBD
  - Constant busy loop: TBD
  - Idle system: TBD
  - Idle system with Ethernet PHY disabled: TBD
  - APM sleep mode with Ethernet PHY disabled: TBD
- **Operating Temperature:** -40 ~ 85° C (-40 ~ 185° F), fan-less operation
- **Operating Humidity:** 0%~90% relative humidity, non-condensing

2.2 Real Time Clock

The SoM-9G25 has an embedded Real-time Clock. Battery backup is provided from the carrier board using the VSTBY pin. The SoM-9G25 will retain the RTT value register during reset and hence use it as a RTC. The RTC has the provision to set Alarms that can interrupt the processor. For example the processor can be placed in sleep mode and then later awakened via the Alarm function.

2.3 Watchdog Timer

The SoM-9G25 has a processor based Watchdog Timer. The Watchdog Timer can be used to prevent system lock-up if the software becomes trapped in a deadlock. It features a 12-bit down counter that allows a watchdog period of up to 16 seconds (slow clock at 32.768 kHz). It can generate a general reset or a processor reset only. In addition, it can be stopped while the processor is in debug mode or idle mode.

2.4 External Connections

The SoM-9G25M connects to a carrier board containing its connectors, power supply and any expansion IO, through a standard gold-plated SODIMM 144 pin edge connector (top-side shown below).

The SoM model will fit in any standard 144-pin SODIMM socket. These connections are designed to be compatible with all EMAC 144-pin SoM products. See EMAC SoM 144-pin SODIMM Pinout Specification to see how other 144-pin SoMs pin-outs line up with the SoM-9G25's pin-out.

The use of the SODIMM form-factor for EMAC's SoMs is a sound choice that has been proven rugged and reliable in the laptop market.

The remainder of this section describes the pin-out as it applies specifically to the SoM-9G25 processor.

2.4.1 External Bus

The SoM-9G25 provides a flexible external bus for connecting external bus peripherals such as the CPLD of the SoM-150ES which connects through a subset of these connections. The Flash WP for the Data Flash is active low and pulled up on-module.

External Bus

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
100	GP_CS1	PD19/NCS2	General Purpose Processor Chip Select CS2
98	GP_CS2	PD20NCS4	General Purpose Processor Chip Select CS4
108	GP_CS3	PD21/NCS5	General Purpose Processor Chip Select CS5
16	~RD/~OE	NRD	Read Signal
83	~WR	NWR0	Write Signal
6	~RST_IN	NRST	Processor Reset In
43	~RST_OUT	SOM_RST_OUT	Processor Reset Out
44	~EA	SHDN	Shutdown Control
85	Flash WP	Serial Flash WP	Data Flash Write Protect
72	ALE/~TS	WKUP	Wake-Up Input
26,35,33,31, 28,109,111, 113,10,12,18, 14,37,5,11,9,7 ,13,97,17, 15,104	A0-A21	A0-A19, A23-A24	Address Bus
29,27,25,22, 23,21,19,20, 8,24,34,70, 77,81,84,86	D0-D15	D0-D15	Data Bus

2.4.2 JTAG

The SoM specifications allow for access to the JTAG lines for the AT91SAM9G25 processor. These connections will allow the Flash to be programmed in circuit via a program running from the processor and also the capability to debug software.

Processor JTAG

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
139	JTAG_TCK	TCK	JTAG clock
137	JTAG_TDI	TDI	JTAG serial in
138	JTAG_TDO	TDO	JTAG serial out
140	JTAG_TMS	TMS	JTAG operation mode
112	JTAG_TRST	NTRST	Test Reset Signal

2.4.3 One-Wire / I2C

The SoM specification calls for a one-wire port. Since the SoM-9G25 does not have a one-wire port, this line is not connected for One-Wire Operation. The 9G25 processor does provide an I2C bus and so these pins are dedicated to that function although they can also be used as GPIOs.

One-Wire / I2C Port

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
116	SCL	TWCK1	One Wire or I^2C Clock
88	SDA	TWD1	I^2C Data

2.4.4 Ethernet

The SoM-9G25 provides a Micrel KSZ8041 Ethernet RMII PHY IC on board. Carrier designers need only run these lines through the appropriate magnetics layer to have a functional Ethernet connection. Remember the RX and TX lines are differential pairs and need to be routed as such.

The LED/configuration pins' state at reset determines the Ethernet's configuration (10-baseT, 100-base-T, autoconfig) and the function of the LED's. The SoM-150ES pull them all high, which configures the chip for network autoconfig, with LED1 functioning as active low link, and LED2 functioning as active low Rx Activity (Refer to Carrier schematics).

The Ethernet PHY can be put into a low power mode by writing directly to the MAC via software.

Additional power can be saved by turning off the PHY Oscillator. This is done by setting GPIO PB17 low. Make sure to send software commands to the PHY to put it into power-down mode before shutting off the Oscillator. When restoring the PHY first turn the Oscillator on before accessing the PHY.

Ethernet

SODIMM Pin#	SoM Pin Name	{PHY} Pin Name	Description
89	LED1_LINK	LINK_LED	Ethernet LED/Configuration pin
90	LED2_ACT	ACTI_LED	Ethernet LED/Configuration pin
94	Ethernet_Rx-	RX_N	Low differential Ethernet receive line
92	Ethernet_Rx+	RX_P	High differential Ethernet receive line
93	Ethernet_Tx-	TX_N	Low differential Ethernet transmit line
91	Ethernet_Tx+	TX_P	High differential Ethernet transmit line

2.4.5 USB

The SoM-9G25 module specific interface brings out several module specific connections from the processor. The interface includes the debug serial port, USB host/device and MMC/SD interfaces. Remember the USB Data lines are differential pairs and need to be routed as such.

USB

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
64	USB1_D+	HHSDB_P	USB Host Port B High Speed Data +
66	USB1_D-	HHSDB_N	USB Host Port B High Speed Data -
65	USB2_D+	HFSDC_P	USB Host Port C Full Speed Data +
67	USB2_D-	HFSDC_N	USB Host Port C Full Speed Data -
60	USB3/OTG_D-	HHSDA/DHSD_N	USB Host/Device High Speed Data -
61	USB3/OTG_D+	HHSDA/DHSD_P	USB Host/Device High Speed Data +
45	USB_OTG_VBUS	PC5/TIOA4	USB Device Port VBUS Detect

2.4.6 SPI

The AT91SAM9G25 processor provides a dual (0 and 1) SPI module for communicating with peripheral devices. The SPI0 bus is connected internally to the serial flash, which uses SPI0_NPCS0

(SPI0_NPCS0 is not brought out to the card fingers). The first Table below lists the lines for the #0 SPI module. While the SoM pin specification allows for three SPI chip selects, there are not three available, so GPIO lines are utilized for SPI slave select line SPI_CS1 and SPI_CS2. The second Table below lists the lines for the #1 SPI module.

Serial Peripheral Interface

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
122	SPI0_MI	SPI0_MISO	SPI0 serial data in
121	SPI0_MO	SPI-_MOSI	SPI0 serial data out
120	SPI0_SCK	SPI0_SCK	SPI0 serial clock out
123	SPI0_CS0	PC16/UTXD1	SPI0 slave select line 0
124	SPI0_CS1	PC17/URXD1	SPI0 slave select 1
110	SPI0_CS2	PC12/TIOA5	SPI0 slave select 2

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
133	SPI1_MISO/GPIO	SPI1_MISO	SPI1 serial data in
134	SPI1_MOSI/GPIO	SPI1_MOSI	SPI1 serial data out
135	SPI1_SCK/GPIO	SPI1_SPCK	SPI1 serial clock out
136	SPI1_NPCS0/GPIO	SPI1_NPCS2	SPI1 slave select line 0
105	SPI1_NPCS1/GPIO	SPI1_NPCS3	SPI1 slave select line 1

2.4.7 MCI Multimedia Card

The AT91SAM9G25 processor provides a 4-bit MMC/SD card interface using the MC lines. MMC/SD MCI0 lines are allocated for SDIO functionality although they can be configured as GPIOs.

The SoM-9G25 could be programmed to use this serial interface, however the drivers provided are written to utilize the 4-bit interface and as such required the SoM-150ES Carrier board to use these drivers.

MMC/SD Card Interface

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
54	MMC_CLK	PA17/MCI0_CLK	MCI0 Clock
51	MMC_CMD	PA16/MCI0_CDA	MCI0 Command
50	MMC_DA0	PA15/MCI0_DA0	MCI0 D0
55	MMC_DA1	PA18/MCI0_DA1	MCI0 D1
56	MMC_DA2	PA19/MCI0_DA2	MCI0 D2
57	MMC_DA3	PA20/MCI0_DA3	MCI0 D3
42	MMC_CD	PC4	Card Detect

2.4.8 Serial Ports

The SoM-144 pin specification has the provision for 5 serial ports. However, the AT91SAM9G25 provides 7 serial ports. The 2 additional serial ports are accommodated through the use of alternate SoM pins. The SoM specification calls for Com0 to be the terminal port, which is the default for both Dallas/Maxim's Tini OS, and µClinux. USART03 on the 9G25 processor provides handshaking pins.

Serial Ports

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
71	COMA_RXD	PC9/URXD0	COMA Receive/GPIO
73	COMA_TXD	PC8/UTXD0	COMA Transmit/GPIO
38	COMB_RXD	RXD0	COMB Receive/GPIO
36	COMB_TXD	TXD0	COMB Transmit/GPIO
82	COMB_RTS/GPIO	RTS0	COMB RTS/GPIO
78	COMB_CTS/GPIO	CTS0	COMB CTS/GPIO
103	COMC_RXD	RXD3	COMC Receive/GPIO
102	COMC_TXD	TXD3	COMC Transmit/GPIO

107	COMC_DSR/GPIO	PC26/SCK3	COMC DSR/GPIO
106	COMC_DTR/GPIO	PC20/PWM2	COMC DTR/GPIO
76	COMC_RI/GPIO	PC21/PWM3	COMC RING/GPIO
30	COMC_DCD/GPIO	PC15/PCK0	COMC DCD/GPIO
39	COMC_RTS/GPIO	RTS3	COMC RTS/GPIO
79	COMC_CTS/GPIO	CTS3	COMC CTS/GPIO

Additional Serial Ports

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
46	Debug RXD	DRXD	Debug Receive/GPIO
47	Debug TXD	DTXD	Debug Transmit/GPIO
49	COMD RXD	RXD2	COMD Receive/GPIO
48	COMD TXD	TXD2	COMD Transmit/GPIO

2.4.9 I2S

I2S

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
87	I2S_CLK/TK	I2S_TK	Transmit Clock
80	I2S_LRCK/TF	I2S_TF	Transmit Frame
125	I2S_TXD/TD	I2S_TD	Transmit Data
126	I2S_RXD/RD	I2S_RD	Receive Data
128	I2S_RF	I2S_RF	Receive Frame
127	I2S_RK	I2S_RK	PA28/TIOB1/RK

2.4.10 GPIO

This section provides for the SoM general purpose IO section. All of these pins can be configured to be general-purpose digital ports. They can also be configured to take advantage of several of the functions of the 9G25's internal silicon. All of the internal A/D ports are brought out here, as well as all of the available IRQs, the second SPI and the pins for general-purpose timer/counters.

Interrupt Lines

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
75	IRQA/GPIO_1	FIQ	Fast Interrupt Request A
32	IRQB/GPIO_2	PC3	Interrupt Request B
40	IRQC/GPIO_0	PC13/TIOB5	Interrupt Request C

A/D:

Analog to Digital Converters

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
129	AD1/GPIO_5	AD0/PWM0	Analog Input 1 / PWM Output 1
130	AD2/GPIO_6	AD1/PWM1	Analog Input 2 / PWM Output 2
131	AD3/GPIO_7	AD2/PWM2	Analog Input 3 / PWM Output 3
132	AD4/GPIO_8	AD3/PWM3	Analog Input 4 / PWM Output 4

Timer/Counters:

Timers/Counters

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
117	CLK1/GPIO_3	TIOA3	Timer Counter IO 3 / GPIO
127	CLK2/GPIO_4	I2S_RK	SSC RX CLK / Timer Counter IO 1 / GPIO
114	PWM1/GPIO_14	PWM0	PWM Output 0 / GPIO
115	PWM2/GPIO_15	PWM1	PWM Output 1 / GPIO

Module Status LED:

General Purpose IO

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
40	IRQC/GPIO_0	PC13/TIOB5	GPIO / Interrupt Request C
75	IRQA/GPIO_1	FIQ	GPIO / Interrupt Request A
32	IRQB/GPIO_2	PC3	GPIO / Interrupt Request B
117	CLK1/GPIO_3	TIOA3	GPIO / Timer Counter IO 3
127	CLK2/GPIO_4	I2S_RK	GPIO / I2S Master Clock
129	AD1/GPIO_5	AD0/PWM0	GPIO / Analog Input 1 / PWM Output 1
130	AD2/GPIO_6	AD1/PWM1	GPIO / Analog Input 2 / PWM Output 2
131	AD3/GPIO_7	AD2/PWM2	GPIO / Analog Input 3 / PWM Output 3
132	AD4/GPIO_8	AD3/PWM3	GPIO / Analog Input 4 / PWM Output 4
133	SPI0_MI/GPIO_9	SPI1_MISO	GPIO / SPI1 Master In Slave Out
134	SPI0_MO/GPIO_10	SPI1_MOSI	GPIO / SPI1 Master Out Slave In
135	SPI0_SCK/GPIO_11	SPI1_SPCK	GPIO / SPI1 Serial Clock
136	SPI0_CS0/GPIO_12	SPI1_NPCS2	GPIO / SPI1 Chip Select 0
105	SPI0_CS1/GPIO_13	SPI1_NPCS3	GPIO / SPI1 Chip Select 1
114	PWM1/GPIO_14	PWM0	GPIO / PWM Output 1
115	PWM2/GPIO_15	PWM1	GPIO / PWM Output 2
48	COMD TXD/GPIO_16	TXD2	GPIO / COMD TX Data
49	COMD RXD/RXD2	RXD2	GPIO / COMD RX Data

2.5 Power Connections

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
3,4,141,142	3.3VCC	3.3VCC	3.3 Volt I/O voltage to the processor
1,2,52,53, 58,59,62,63,68,69,143, 144	GND	GND	Ground
119	VSTBY	VDDBU	Voltage standby, this is the backup voltage provided to the internal RTC of the processor. If RTC readings are not important for and application, this can be attached to the 3.3V rail.
118	ALT_VCC	Not Used	Not Required
101	AV_VCC	Not Used	Analog power is not required for the SoM-9G25
99	V_REF	Not Used	No external Analog Reference voltage is required for the SoM-9G25.

2.6 Boot Options

The SoM specification provides two pins for boot time configuration. On the SoM-9G25, these are BMS and Flash Disable. The Boot Mode Select (BMS) pin allows the SoM-9G25 to low-level booted from either its internal ROM or external (carrier resident) NOR flash.

The Flash Disable pin should be tied to GND to enable the Serial Data Flash .

The Module can high-level boot from either the Serial Data Flash or the eMMC Flash (selected through the low-level bootloader). It is recommended to high-level boot from the Serial Data Flash, as this Flash is more reliable than the eMMC Flash.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
41	BOOT_OPTION1	BMS	Boot Mode Select
74	BOOT_OPTION2	Flash Disable	Serial Data Flash Disable

2.7 Serial Data Flash

The Serial Data Flash is connected to SPI0 and uses SPI0_NPCS0 to enable it. The Serial Data Flash also has a Write Protect Provision. To Write Protect the Serial Data Flash pull SoM pin# 85 low. SoM pin# 85 is pulled up by a 4.7K ohm resistor on the module.

If this feature is required it would be implemented on the carrier as a jumper or an I/O line.

3 Design Considerations

One of the goals of the SoM-9G25 is to provide a modular, flexible and inexpensive solution capable of delivering high-end microcontroller performance with low power requirements.

3.1 Power

The SoM-9G25 requires a voltage of 3.3V at ~300mA. For a bare-bones population, users can get away with using only 3.3V, and simply provide this to all the voltage inputs listed in Power Connections section. This however, will not provide battery backup for the RTC or 5V for the USB Host ports

3.1.1 Legacy

ALT_VCC is a legacy connection, required to support the SoM-400EM and may be used in future SoM modules. If general SoM compatibility is not an issue then this can be tied to 3.3V. The SoM-9G25 does not use this connection.

3.1.2 Analog Reference

No external Analog Reference voltage (VREF) is required for the SoM-9G25. An on-module 2.5V reference is provided. Analog input range is therefore 0 to 2.5V. This pin is normally a No Connect on the Module. This Reference uses power and therefore can be turned off by setting GPIO Port Line PB16 to a high, thus conserving about 3 ma.

3.1.3 Shutdown Logic Pins

The SHDN is a digital output only with a logical high of 3.3V, which is driven by the Shutdown Controller on the processor.

The WKUP pin has a Maximum input voltage of 3.3V.

Both of these pins are connected directly to the processor.

3.1.4 Battery Backup

The SoM-9G25 contains 3 potentially non-volatile memory areas, the real time clock, and the serial flash of the processor. The serial flash is always non-volatile, the real time clock requires a backup voltage to maintain its data. This backup voltage comes from the VSTBY pin, and should be connected to 3.3 volts.

The RTC will draw approximately 10 uA when the processor is not powered by the 3.3V supply. The Static current can rise to 18uA if the temperature increases to 85° C. When the module is powered no current is drawn from the backup battery supply. If the RTC is not needed, this can be tied to 3.3V.

The SoM-150ES provide battery backup voltage through a socketable BR2032, which is a standard 3V 190mA/H 20MM coin battery that can be picked up from most electronics stores.

3.1.5 Analog Voltage

When designing power for the Analog subsystem there are 2 major considerations, range and accuracy.

- **Range**

  The AV_VCC pin normally provides the range. However on the SoM-9G25 the Analog VCC (VDDANA) is directly connected to filtered 3.3V. The power supplied to the analog subsystem limits the range of voltages that can be accurately measured. The internal analog converters cannot measure a voltage higher than their power rail. The Analog input range is 0 to 2.5V.

- **Accuracy**

  The accuracy of the A/D converters is determined by the V_REF pin, which provides the reference voltage to the analog subsystem. The stability of the voltage between this pin and ground will affect the accuracy of the subsystem's measurements. No external Analog Reference voltage is required for the SoM-9G25. An on-module 2.5V reference is provided. Analog input range is therefore 0 to 2.5V.

4 Software

The SoM-9G25 offers a wide variety of software support from both open source and proprietary sources. The hardware core was designed to be software compatible with the Atmel AT91SAM9G25 reference design, which is supported by Linux.

4.1 Qt Creator

Qt Creator is a cross-platform IDE (Integrated Development Environment) tailored to the needs of Qt developers but works well for Headless applications as well. EMAC provides sample code for the SoM-9G25 as projects that can be imported into Qt Creator. Qt Creator supports remote deployment and source debugging.

https://qt-project.org/wiki/Category:Tools::QtCreator

4.2 Das U-Boot

The SoM-9G25 is distributed with Das U-Boot installed. U-Boot is an open source/cross-architecture platform independent bootloader. It supports reading and writing to the flash, auto-booting, environmental variables, and TFTP. Das U-boot can be used to upload and run and/or reflash the OS on the SoM-9G25 or to run stand-alone programs without an OS. SoM-9G25 modules are shipped with a valid MAC address installed in flash in the protected U-boot environmental variable “ethaddr”. At boot time U-Boot automatically stores this address in a register within the MAC, which effectively provides it to any OS loaded after that point.

4.3 Embedded Linux

EMAC Open Embedded Linux is an open source Linux distribution for use in embedded systems. This Linux build for the SoM-9G25 is based on the Open Embedded (www.openembedded.org) Linux build system. The current kernel is Linux 3.10.0 or higher patched to support the SoM-9G25. Open Embedded is a superior Linux distribution for embedded systems. Custom Linux builds are also available on request.

The distribution contains everything a user could expect from a standard Linux kernel: powerful networking features, advanced file system support, security, debugging utilities, and countless other features.

The basic root file system includes:

- Busybox
- Hotplugging support
- APM utilities for power management
- Openssh SSH server
- lighttpd HTTP server

- EXT4 file system with utilities

The SoM-9G25 will work out of the box with EMAC's preinstalled Embedded Linux distribution.

4.3.1 EMAC OE Linux Wiki

EMAC provides a wiki to help support our hardware with EMAC OE Linux. The wiki can be accessed at:

http://wiki.emacinc.com/wiki/Main_Page

4.3.2 Linux with Xenomai Real Time Extensions

Xenomai provides real time extensions to the kernel and can be used to schedule tasks with hard deadlines and μs latencies. The Xenomai build is an additional module that can be added to the standard Linux kernel and is available for a one-time inexpensive support/installation fee.

http://www.xenomai.org/

4.3.3 Linux Modules

EMAC provides support for many Linux modules such as: Lighttpd Web Server, PHP, SQLite, Perl, SNMP, DHCP Server, etc. As with the Xenomai module, other modules can be added to the standard Linux file system and are available for a one-time inexpensive support/installation fee.

4.3.4 Linux Patches

In addition to standard Embedded Linux support, EMAC has released a number of patches and device drivers from the open source community and from internal EMAC engineering into its standard distribution.

Along with kernel patches, EMAC provides the binaries for the kernel and root file system.

4.4 ARM EABI Cross Compiler

The popular open source gcc compiler has a stable build for the ARM family. EMAC uses the 4.9.1 version of the ARM EABI compiler. The Embedded Linux kernel and EMAC Qt Creator projects use this compiler for building ARM stand alone, and OS specific binaries. The EMAC Qt Creator provides source level debugging over Ethernet or serial using gdbserver. The Linux binaries for the ARM EABI cross compiler are available online along with the SDK for the SoM-9G25 at the following location.

ftp://ftp.emacinc.com/Controllers/SoM/SoM-9G25/Tools/