SoM-9G20M

User Manual

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1. Introduction

This document describes EMAC's SoM-9G20M (SBC) module. The SoM-9G20M is a System on Module, designed to be compatible with EMAC's 144-pin SODIMM form factor. This module is built around the ATMEL AT91SAM9G20 microcontroller, which provides several of its key features.

The SoM-9G20M has an onboard Ethernet PHY, 7 serial ports (one of which is optional), a RTC, a programmable clock synthesizer, onboard NAND flash, Serial EEPROM, and SDRAM.

In addition to these standard SoM features, the SoM-9G20M also features a fast 32-bit core, open source software support, and a wide range of controller IO pins.

1.1. Features

- **Small, 144 pin SODIMM form factor (2.66" x 1.5")**
- **Atmel ARM9 Jazelle AT91SAM9G20 400Mhz Processor**
- **10/100BaseT Ethernet with on-board PHY**
- **6 Serial ports, one with full handshake and three with CTS/RTS handshake (an additional serial port can be had, 7 total as an option)**
- **2 USB 2.0 (Full Speed) Host ports**
- **1 USB 2.0 (Full Speed) Device port**
- **Up to 64 MB of SDRAM**
- **Up to 1 GB of Resident NAND Flash**
- **128K Bytes of Serial Flash**
- **Battery backed Real Time Clock**
- **SD/MMC Flash Card Interface**
- **2 SPI ports**
- **1 I2S Audio port**
- **Image Sensor Interface (ISI), ITU-R BT 610/656**
- **Timer/Counters and Pulse Width Modulation (PWM) ports**
- **4 Channel 10-bit Analog-to-Digital converter**
- **Typical power requirement less than 1 Watt**

- **JTAG for debug, including real-time trace**
- **FREE Eclipse IDE with GCC and GDB development tools**
- **WinCE 6.0 BSP in development.**

2. Hardware

2.1. Specifications

- **CPU:** Embedded Atmel AT91SAM9G20 processor running at 400 MHz.
- **Flash:** 256 MB NAND Flash and 4MB of Serial Data Flash.
- **RAM:** 16 MB 133 MHz SDRAM.
- **Flash Disk:** 4-bit Parallel or SPI serial SDHC/MMC interface.
- **System Reset:** Supervisor with external Reset Button provision.
- **RTC:** Real Time Clock/Calendar with battery backed provision using 32-bit free running counter.
- **Timer/Counters:** 2, 3 channel, 16-bit timers/counters with capture, compare, and PWM. 20-bit interval timer plus 12-bit interval counter.
- **Watchdog Timer:** External Watchdog Timer (MAX6747).
- **Digital I/O:** 32 General Purpose I/Os with 16 mA drive when used as an output
- **Analog I/O:** 4 channel, 10-bit Analog-to-Digital converter (ADC)
- **Power:** Power Management Controller allows selectively shutting down on processor I/O functionality and running from a slow clock.
- **JTAG**: JTAG for debug, including real-time trace
- **CLOCKS**: PLL synthesized 8M, 200K, 14.3M clock outputs

Serial Interfaces

- **UARTS:** 6 serial TTL level serial ports with Auto RS485 and some with handshaking (each UART requires external RS level shifting).
- **SPI:** 2 High-Speed SPI ports with Chip Selects.
- **Audio:** I2S Synchronous Serial Controller with analog interface support
- **USB:** Dual USB 2.0 Full Speed Host and single USB 2.0 Full Speed Device ports

Ethernet Interface

- **MAC:** AT91SAM9G20 on chip MAC
- **PHY:** Micrel KSZ8041 with software PHY shutdown control
- **Interface:** IEEE 802.3u 10/100 BaseT Fast Ethernet (requires external magnetics and Jack)

Bus Interface

- Local ARM AT91SAM9G20 Bus accessible through SODIMM provides 22 address lines, 16 data bus lines, and control lines.

Mechanical and Environmental

- **Dimensions:** SODIMM form factor with the length dimension extended (2.66" x 1.5")
- **Power Supply Voltage:** +3.3 Volts DC +/- 5%
- **Power Requirements (32MB SoM):**
  - Typical 3.3 Volts @ 175 mA (less than 1 watt)
  - Max current draw during boot process: 240 mA
  - Constant busy loop: 215 mA
  - Idle system: 180 mA
  - Idle system with Ethernet PHY disabled: 65 mA
  - APM sleep mode with Ethernet PHY disabled: 20 mA
  - APM sleep mode with Ethernet PHY enabled: 115 mA
- **Operating Temperature:** -40 ~ 85° C (-40 ~ 185° F), fan-less operation
- **Operating Humidity:** 0%~90% relative humidity, non-condensing

2.2. Real Time Clock

The SoM-9G20M emulates a real time clock using the AT91SAM9G20's onboard real time timer. Battery backup is provided from the carrier board using the VSTBY pin. The SoM-9G20M will retain the RTT value register during reset and hence use it as a RTC. The RTC has the provision to set Alarms that can interrupt the processor. For example the processor can be placed in sleep mode and then later awakened via the Alarm function.

2.3. Watchdog Timer

The internal Watchdog Timer provide with the AT91SAM9G20 is not very functional due to the fact that it cannot be reprogrammed. The SoM-9G20M therefore provides an external Watchdog Timer/ Supervisor (MAX6747) with an extended watchdog timeout period of 1.42 seconds (±10%). Upon power-up the Watchdog is disabled and does not require pulsing. To start the Watchdog it must first be enabled. This is done by configuring port line PA27 as an output and setting it low in software. Once enabled, the Watchdog should be pulsed, using port line PB20, continually every 1.28 seconds or faster to prevent the Watchdog from timing out and resetting the module. If you are using the watchdog to force a system reset, you may need up to 1.56 seconds of inactivity before the Watchdog reset will occur. The watchdog is automatically disabled upon reset but it can also be disabled by setting PA27 high.

2.4. External Connections

The SoM-9G20M connects to a carrier board containing its connectors, power supply and any expansion IO, through a standard gold-plated SODIMM 144 pin connection (top half shown below).

The SoM model will fit in any standard 144-pin SODIMM socket. These connections are designed to be compatible with all EMAC 144-pin SoM products. See EMAC SoM 144-pin SODIMM Pinout Specification to see how other 144-pin SoMs pin-outs line up with the SoM-9G20's pin-out.

The use of the SODIMM form-factor for EMAC's SoMs is a sound choice that has been proven rugged and reliable in the laptop market.

The remainder of this section describes the pin-out as it applies specifically to the SoM-9G20M processor.

2.4.1. External Bus

The SoM-9G20M provides a flexible external bus for connecting peripherals. The CPLD of the SoM-100ES and SoM-150ES connect through a subset of these connections. The WKUP pin has a Maximum input voltage of 1.0V (pulled up on-module to 1.0V) and Shutdown has a maximum output voltage of 1.0V. The Flash WP for the Data Flash is active low and pulled up on-module.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
100	GP_CS1	NCS0	General Purpose Processor Chip Select CS0
98	GP_CS2	PC9/NCS5/TIOB0	General Purpose Processor Chip Select CS5
108	GP_CS3	NCS4/RTS3/PC8	General Purpose Processor Chip Select CS4
16	~OE	NRD	Read Signal
83	~WR	NWR0/NWE	Write Signal
6	~RST_IN	NRST	Processor Reset
43	~RST_OUT	NRST	Processor Reset
44	~EA	SHDN	Shutdown Control
85	Flash WP	Data Flash WP	Data Flash Write Protect
72	ALE/~TS	WKUP	Wake-Up Input
26,35,33,31, 28,109,111, 113,10,12,18, 14,37,5,11,9, 7,13,97,17, 15,104	A0-A21	A0-A18, A23-A25	Address Bus
29,27,25,22, 23,21,19,20, 8,24,34,70, 77,81,84,86	D0-D15	D0-D15	Data Bus

2.4.2. Module specific interface

The SoM-9G20M module specific interface brings out several module specific connections from the processor. The interface includes the debug serial port, USB host/device and MMC/SD interfaces. Remember the USB Data lines are differential pairs and need to be routed as such.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
45	MS0	PCK1/PB31	Programmable Clk Output/GPIO
46	MS1	DRXD/PB14	Debug RX/GPIO
47	MS2	DTXD/PB15	Debug TX/GPIO
48	MS3	TXD5/PB12	SER5 TX/GPIO
49	MS4	RXD5/PB13	SER5 RX/GPIO
50	MS5	MCDA0/PA6	MCI A Data0/GPIO
51	MS6	MCCDA/PA7	MCI A Command/GPIO
54	MS7	MCCK/PA8	MCI Clock/GPIO
55	MS8	MCDA1/PA9	MCI A Data1/GPIO
56	MS9	MCDA2/PA10	MCI A Data2/GPIO
57	MS10	MCDA3/PA11	MCI A Data3/GPIO
60	MS11	DDM (USBD)	Device USB
61	MS12	DDP (USBD)	Device USB
64	MS13	HDPA (USBH)	HostA USB
65	MS14	HDPB (USBH)	HostB USB
66	MS15	HDMA (USBH)	HostA USB
67	MS16	HDMB (USBH)	HostB USB

2.4.3. JTAG

The SoM specifications allows for access to the JTAG lines for the AT91SAM9G20 processor. These connections will allow the Flash to be programmed in circuit via a program running from the processor and also the capability to debug software.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
139	JTAG_TCK	JTAG_TCK	JTAG clock -> port B0
137	JTAG_TDI	JTAG_TDI	JTAG serial in -> port B1
138	JTAG_TDO	JTAG_TDO	JTAG serial out ->port B2
140	JTAG_TMS	JTAG_TMS	JTAG operation mode ->port B3
112	JTAG_TRST	JTAG_NTRST	Test Reset Signal

2.4.4. One-Wire/I2C

The SoM specification calls for a one-wire port. Since the SoM-9G20M does not have a one-wire port, this line is not connected for One-Wire Operation. The 9G20 processor does provide an I2C bus and so these pins are dedicated to that function although they can also be used as GPIOs.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
116	LOCAL1W/SCL	PA24/TWCK	I2C Clock
88	SDA	PA23/TWD	I2C Data

2.4.5. Ethernet

The SoM-9G20M provides a Micrel KSZ8041 Ethernet RMII PHY IC on board. Carrier designers need only run these lines through the appropriate magnetics layer to have a functional Ethernet connection. Remember the RX and TX lines are differential pairs and need to be routed as such.

The LED/configuration pins' state at reset determines the Ethernet's configuration (10-baseT, 100-base-T, autoconfig) and the function of the LED's. The SoM-100ES and the SoM-150ES pull them all high, which configures the chip for network autoconfig, with LED1 functioning as active low link, and LED2 functioning as active low Rx Activity (Refer to Carrier schematics).

The Ethernet PHY can be put into a low power mode by writing directly to the MAC via software. Additional power can be saved by turning off the PHY Oscillator. This is done by setting GPIO PA25 low. Make sure to send software commands to the PHY to put it into power-down mode before shutting off the Oscillator. When restoring the PHY first turn the Oscillator on before accessing the PHY.

SODIMM Pin#	SoM Pin Name	LXT972 Pin Name	Description
89	LED_LINK/ CFG_1	LED_LINK/ CFG_1	Ethernet LED/Configuration pin
90	LED_RX/ CFG_2	LED_RX/ CFG_2	Ethernet LED/Configuration pin
94	Ethernet_Rx-	Ethernet_Rx-	Low differential Ethernet receive line
92	Ethernet_Rx+	Ethernet_Rx+	High differential Ethernet receive line
93	Ethernet_Tx-	Ethernet_Tx-	Low differential Ethernet transmit line
91	Ethernet_Tx+	Ethernet_Tx+	High differential Ethernet transmit line

2.4.6. SPI

The AT91SAM9G20 processor provides a dual (0 and 1) SPI module for communicating with peripheral devices. The SPI0 bus is connected internally to the serial flash, which uses SPI0_NPCS1 (SPI0_NPCS1 is not brought out to the card fingers). The first Table below lists the lines for the #0 SPI module. While the SoM pin specification allows for three SPI chip selects, there are not three available, so GPIO lines are utilized for SPI slave select line SPI_CS1 and SPI_CS2. The second Table below lists the lines for the #1 SPI module.

The SPI pins listed below also can be configured in software as a 4-bit MMC/SD card interface using the MC lines. The AT91SAM9G20 processor provides a dual (A and B) MMC/SD SPI module. The MMC/SD B interface lines are listed in the MCI Multimedia Card Table further below.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
122	SPI_MI	SPI0_MI/PA0/MCDB0	SPI0 serial data in
121	SPI_MO	SPI0_MO/PA1/MCCDB	SPI0 serial data out
120	SPI_SCK	SPI0_SCK/PA2	SPI0 serial clock out
123	SPI_CS0	SPI0_CS0/PA3/MCDB3	SPI0 slave select line 0
124	SPI_CS1	PA4/RTS2/MCDB2	SPI0 slave select line 1
110	SPI_CS2	PA5/RTS2/MCDB1	SPI0 slave select line 2

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
133	GPIO12	SPI1-MI/TIOA3/PB0	SPI1 serial data in
134	GPIO13	SPI1-MO/TIOB3/PB1	SPI1 serial data out
135	GPIO14	SPI1-SPCK/TIOA4/PB2	SPI1 serial clock out
136	GPIO15	SPI1-CS0/TIOA5/PB3	SPI1 slave select line 0
15	A20	A24/SPI1_CS1/PC5	SPI1 slave select line 1
17	A19	A23/SPI1_CS2/PC4	SPI1 slave select line 2
132	GPIO11	AN3/SPI1-CS3/PC3	SPI1 slave select line 3

Note: A24/SPI1_CS1 and A23/SPI1_CS2 are used for addressing. However, since the SoM-9G20 uses NAND Flash these lines are not used by the module and are free to use.

2.4.7. MCI Multimedia Card

The AT91SAM9G20 processor provides a dual 4-bit MMC/SD card interface using the MC lines. The MMC/SD B lines are shared with SPI0 lines, however they can be used in both functions with software arbitration.

The SoM-100ES Carrier board uses a serial SPI based MMC/SD interface. The SoM-9G20 could be programmed to use this serial interface, however the drivers provided are written to utilize the 4-bit interface and as such required the SoM-150ES Carrier board to use these drivers.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
54	MS7	MCCK/PA8	MCI Clock
51	MS6	MCCDA/PA7	MCIA Command
50	MS5	MCDA0/PA6	MCIA D0
55	MS8	MCDA1/PA9	MCIA D1
56	MS9	MCDA2/PA10	MCIA D2
57	MS10	MCDA3/PA11	MCIA D3

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
54	MS7	MCCK/PA8	MCI Clock
121	SPI_MO	SPI0_MO/PA1/MCCDB	MCIB Command
122	SPI_MI	SPI0_MI/PA0/MCDB0	MCIB D0
110	SPI_CS2	PA5/CTS2/MCDB1	MCIB D1
124	SPI_CS1	PA4/RTS2/MCDB2	MCIB D2
123	SPI_CS0	SPI0_CS0/PA3/MCDB3	MCIB D3

Note: Both the MCI A and B interfaces share the same CLK line.

2.4.8. Serial Ports

The SoM-144 pin specification has the provision for 3 serial ports. However, the AT91SAM9G20 provides 7 serial ports. The SoM-9G20M provides 6 serial ports with the seventh available optionally. The 4 additional serial ports are accommodated through the use of alternate SoM pins. Typically, the SoM specification calls for Com0 to be the terminal port, which is the default for both Dallas/Maxim's Tini OS, and μClinux. However, USART0 on the 9G20 processor provides handshaking pins, which go to waste on a terminal port. For this reason, the default Linux serial console for the SoM-9G20M is USART3, which is routed to COMA in the EMAC SoM specification. WinCE however uses the Debug serial port as its default console, which is routed to COME (SoM pins 46 & 47).

SoM Defined Serial Lines

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
71	COMA_RXD	RXD3/PB11	SER3 receive/GPIO
73	COMA_TXD	TXD3/PB10	SER3 transmit/GPIO
38	COMB_RXD	RXD1/PB7	SER 1 receive/GPIO
36	COMB_TXD	TXD1/PB6	SER 1 transmit/GPIO
82	COMB_RTS/GPIO	RTS1/PB28	SER 1 RTS/GPIO
78	COMB_CTS/GPIO	CTS1/PB29	SER 1 CTS/GPIO
103	COMC_RXD	RXD0/PB5	SER 0 receive/GPIO
102	COMC_TXD	TXD0/PB4	SER 0 transmit/GPIO
107	COMC_DSR/GPIO	DSR0/PB22	SER 0 DSR /GPIO
106	COMC_DTR/GPIO	DTR0/PB24	SER 0 DTR/GPIO
76	COMC_RI/GPIO	RI0/PB25	SER 0 RING/GPIO
30	COMC_DCD/GPIO	DCD0/PB23	SER 0 DCD/GPIO
39	COMC_RTS/GPIO	RTS0/PB26	SER 0 RTS/GPIO
79	COMC_CTS/GPIO	CTS0/PB27	SER 0 CTS/GPIO

Note: Pin 30 (COMC_DCD) is output only due to processor Errata. This line utilizes an inverter between the processor and Pin 30 of the SoM. The SoM-9260 does not provide this inverter.

Alternate Serial Lines

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
46	MS1	DRXD/PB14	Debug receive/GPIO
47	MS2	DTXD/PB15	Debug transmit/GPIO
95	CANRX	RXD2/PB9	SER 2 receive/GPIO
96	CANTX	TXD2/PB8	SER 2 transmit/GPIO
110	SPI_CS2	PA5/CTS2/MCDB1	SER 2 RTS/GPIO
124	SPI_CS1	PA4/RTS2/MCDB2	SER 2 CTS/GPIO
108	GP_CS3	NCS4/RTS3/PC8	SER 3 RTS/GPIO
104	A21	A25/CTS3/PC10	SER 3 CTS/GPIO
101	AV_VCC	PA30/RXD4*	SER 4 receive/GPIO
99	V_REF	PA31/TXD4*	SER 4 transmit/GPIO
49	MS4	RXD5/PB13	SER 5 receive/GPIO
48	MS3	TXD5/PB12	SER 5 transmit/GPIO

Note: RTS3 is shared with NCS4, which is used as the chip select for the PLD on the SoM-150ES carrier board. RXD4 & TXD4 require zero ohm resistors installed in order to be functional. These resistors are not installed by default to assure compatibility with other modules.

2.4.9. GPIO

This section provides for the SoM general purpose IO section. All of these pins can be configured to be general-purpose digital ports. They can also be configured to take advantage of several of the functions of the 9G20's internal silicon. All of the internal A/D ports are brought out here, as well as all of the available IRQs, the second SPI and the pins for general-purpose timer/counters.

Interrupts:
The AT96SAM9G20 is capable of using any GPIO pin as an interrupt as well as the pins that are labeled IRQ.

A/D:
The AT96SAM9G20 Analog to Digital pins provides 4 channels of 10-bit resolution with a 4us conversion time. With the enhanced DSP extensions, this can make quite a capable signal processor.

Timer/Counters:
The general-purpose Timer/Counter (TC) module on the AT91SAM9G20 is comprised of three 16-bit timers/counters with independently programmable input-capture or output compare lines. These can be used for a wide variety of timed applications, including counters and PWM.

For more information on the AtoD and Timer functions of the AT91SAM9G20 processor, users are referred to the TC section of the AT91SAM9G20 *User's Manual*.

Module Status LED:
A Green general purpose Status LED is connected to RK0/PB20. The RK0/PB20 processor pin is also GPIO6 (SoM pin# 127). Note: the Module Status LED is shared with the Watchdog Pulse line. If this LED is turned on or off and the Watchdog is enabled care should be taken.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
75	IRQA/GPIO	IRQ0/NCS7/PC12	Fast IRQ/GPIO
32	IRQB/GPIO	IRQ1/PC15	GP IRQ 1/GPIO
40	IRQC/GPIO0	NC	
42	IRQD/GPIO1	PA29/SCK1	GP IRQ /Serial CLK/GPIO
87	IRQE/GPIO2	TK0/TCLK3/PB16	SSC TX CLK/TC Ext CLK/GPIO
80	IRQF/GPIO3	TF0/TCLK4/PB17	SSC TX Sync/TC Ext CLK/GPIO
125	GPIO4	TD0/TIOB4/PB18	SSC TX Data/TC Chan I/O/GPIO
126	GPIO5	RD0/TIOB5/PB19	SSC RX Data/TC Chan I/O/GPIO
127	GPIO6	RK0/PB20	SSC RX CLK/GPIO
128	GPIO7	RF0/PB21	SSC RX Sync/GPIO
129	GPIO8	AN0/PC0	Analog Input/GPIO
130	GPIO9	AN1/PC1	Analog Input/GPIO
131	GPIO10	AN2/PC2	Analog Input/GPIO
132	GPIO11	AN3/SPI1-CS3/PC3	Analog Input/SPI CS/GPIO
133	GPIO12	SPI1-MI/TIOA3/PB0	SPI Data In/ TC Chan I/O/GPIO
134	GPIO13	SPI1-MO/TIOB3/PB1	SPI Data Out/ TC Chan I/O/GPIO
135	GPIO14	SPI1-SPCK/TIOA4/PB2	SPI CLK/ TC Chan I/O/GPIO
136	GPIO15	SPI1-CS0/TIOA5/PB3	SPI CS/ TC Chan I/O/GPIO
105	~LDAC/~GPIO	PCK0/PB30	Prog CLK Out/GPIO
114	8MHz	TIOB2/PC6	TC Chan I/O/GPIO
115	200KHz	TIOB1/PC7	TC Chan I/O/GPIO
117	14.3MHz	TIOA0/PA26	TC Chan I/O/GPIO

2.5. Power Connections

The SoM-9G20M requires a 3.3V supply for the Bus and I/O voltages. The 1.0V core voltage is regulated on module from the 3.3V. The on processor RTC also requires 1.0V and is also regulated down from the 3.3V VSTBY pin. Unlike some other modules no other supply voltage other than 3.3V is required.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
3,4,141,142	3.3VCC	3.3VCC	3.3 Volt I/O voltage to the processor
1,2,52,53, 58,59,62,63, 68,69,143,1, 144	GND	GND	Ground
119	VSTBY	VDDBU battery backup	Voltage standby, this is the backup voltage provided to the internal RTC of the processor. If RTC readings are not important for the application, this can be attached to the 3.3V rail.
118	ALT_VCC	Not Used	Not Required
101	AV_VCC	Not Used	Analog power. This is not required for the SoM-9G20M Note: This pin can be factory configured to allow access to PA30/RXD4.
99	V_REF	Not Used	No external Analog Reference voltage is required for the SoM-9G20. An on-module 2.5V reference (ADR535BRT) is provided. Analog input range is therefore 0 to 2.5V. Note: This pin can be factory configured to allow access to PA31/TXD4.

2.6. Boot Options

The SoM specification provides two pins for boot time configuration. On the SoM-9G20M, these are BMS and Flash Disable. The Boot Mode Select (BMS) pin allows the SoM-9G20 to low-level booted from either its internal ROM or external (carrier resident) NOR flash.

The Flash Disable pin should be tied to GND to enable the Serial Data Flash and the NAND Flash.

The Module can high-level boot from either the Serial Data Flash or the NAND Flash (selected through the low-level bootloader). It is recommended to high-level boot from the Serial Data Flash, as this Flash is more reliable than the NAND Flash. The NAND flash is ideal for the Operating System's File System which can normally mark bad blocks.

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
41	BOOT_OPTION1	BMS	Boot Mode Select
74	BOOT_OPTION2	Flash Disable	NAND Flash Disable Serial Data Flash Disable

2.7. Serial Data Flash

The Module can high-level boot from either the Serial Data Flash or the NAND Flash (selected through the low-level bootloader). It is recommended to high-level boot from the Serial Data Flash, as this Flash is more reliable than the NAND Flash. The NAND flash is ideal for the Operating System's File System which can normally mark bad blocks.

The Serial Data Flash is connected to SPI0 and uses SPI0_NPCS1 to enable it. The Serial Data Flash also has a Write Protect Provision. To Write Protect the Serial Data Flash pull SoM pin# 85 low. SoM pin# 85 is pulled up by a 10K ohm resistor on the module.

If this feature is required it would be implemented on the carrier as a jumper or an I/O line.

3. Design Considerations

One of the goals of the SoM-9G20 is to provide a modular, flexible and inexpensive solution capable of delivering high-end microcontroller performance.

3.1. The EMAC SoM Carrier-SoM-150ES

EMAC provides an off the shelf carrier for the SoM-9G20 module, the SoM-150ES, which provides power to SoM modules and provides them with an extended range of I/O. This board comes with full schematics and BOM, and can be used as is, or as a reference for a customer's own design.

http://www.emacinc.com/som/som150es.htm

EMAC also offers a semi-custom engineering service. By modifying an existing design, EMAC can offer quick-turn, low-cost engineering, for your specific application.

3.2. The EMAC SoM Carrier-SoM-100ES

EMAC provides an off the shelf carrier for it's SoM modules, the SoM-100ES, which provides power to SoM modules and provides them with an extended range of I/O. This board can be used in conjunction with the SoM-9G20, however the Carrier does not provide USB. Additionally, the MMC/SD Flash interface will not work with the provided 4-bit drivers.

http://www.emacinc.com/som/som100es.htm

3.3. Power

The SoM-9G20M requires a voltage of 3.3V at 225mA. For a bare-bones population, users can get away with using only 3.3V, and simply provide this to all the voltage inputs listed in Power Connections section. This however, will not provide battery backup for the RTC. Additionally, 5V is required if USB Host capability is required.

3.3.1. Legacy

ALT_VCC is a legacy connection, required to support the SoM-400EM and may be used in future SoM modules. If general SoM compatibility is not an issue then this can be tied to 3.3V. The SoM-9G20 does not use this connection.

3.3.2. Analog Reference

No external Analog Reference voltage (VREF) is required for the SoM-9G20. An on-module 2.5V reference (ADR535BRT) is provided. Analog input range is therefore 0 to 2.5V. This pin is normally a No Connect on the Module. This Reference uses power and therefore can be turned off by setting GPIO Port Line PA22 to a high, thus conserving about 3 ma.

Note: This pin can be factory configured to allow access to PA31/TXD4.

3.3.3. Shutdown Logic Pins

The SHDN is a digital output only (0 to 1.0V, pulled up on-module), which is driven by the Shutdown Controller on the processor.

The WKUP pin has a Maximum input voltage of 1.0V.

Both of these pins are connected directly to the processor.

3.3.4. Battery Backup

The SoM-9G20M contains 3 potentially non-volatile memory areas, the NAND flash, the real time clock, and the serial flash of the processor. The flash is always non-volatile, the real time clock requires a backup voltage to maintain its data. This backup voltage comes from the VSTBY pin, and should be connected to 3.3 volts.

The RTC will draw approximately 10 uA when the processor is not powered by the 3.3V supply. The Static current can rise to 18uA if the temperature increases to 85° C. When the module is powered no current is drawn from the backup battery supply. If the RTC is not needed, this can be tied to 3.3V.

The SoM-100ES and SoM-150ES provide battery backup voltage through a socketable BR2032, which is a standard 3V 190mA/H 20MM coin battery that can be picked up from most electronics stores.

3.3.5. Analog Voltage

When designing power for the Analog subsystem there are 4 major considerations, range and accuracy output drive, and rise time.

- **Range**
  The AV_VCC pin normally provides the range. However on the SoM-9G20M the Analog VCC (VDDANA) is directly connected to filtered 3.3V. The power supplied to the analog subsystem limits the range of voltages that can be accurately measured. The internal analog converters cannot measure a voltage higher than their power rail. The Analog input range is 0 to 2.5V. Note: This pin can be factory configured to allow access to PA30/RXD4.

- **Accuracy**
  The accuracy of the A/D converters is determined by the V_REF pin, which provides the reference voltage to the analog subsystem. The stability of the voltage between this pin and ground will affect the accuracy of the subsystem's measurements. No external Analog Reference voltage is required for the SoM-9G20. An on-module 2.5V reference (ADR535BRT) is provided. Analog input range is therefore 0 to 2.5V.

4. Software

The SoM-9G20M offers a wide variety of software support from both open source and proprietary sources. The hardware core was designed to be software compatible with the Atmel AT91SAM9G20-EK reference design, which is supported by Linux and WinCE 6.0.

4.1. Eclipse

EMAC provides sample code for the SoM-9G20M as CDT projects within the free Eclipse IDE. Eclipse is a powerful open-source Java based IDE. It has plug-ins for development and debugging in Java and C, as well as several other languages.

http://www.eclipse.org/

EMAC offers a free download of Eclipse pre-integrated with the CDT plug-in and plug-ins for remote debugging and SVN. Eclipse requires the Java Runtime Environment to be installed on the development system. Currently EMAC only supports the use of Eclipse under the Linux environment for the SoM-9G20M. The Eclipse environment and JRE for Linux are available online along with user manuals.

ftp://ftp.emacinc.com/PCSBC/Development_Kits/EMAC_Open_Tools/

4.1.1. Eclipse CDT plug-in

The Eclipse CDT plug-in provides a powerful graphical IDE for C development. This plug-in relies on GNU Make to build its files, so its projects are highly portable to other IDE's (or lack of them completely). It also offers a MI based debugger, for plugging into newer gdbs.

http://www.eclipse.org/cdt/

4.2. Das U-Boot

The SoM-9G20 is distributed with Das U-Boot installed. U-Boot is an open source/cross-architecture platform independent bootloader. It supports reading and writing to the flash, auto-booting, environmental variables, and tftp. Das U-boot can be used to upload and run and/or reflash the OS on the SoM-9G20 without the use of a JTAG cable, or to run stand-alone programs without an OS. SoM-9G20 modules are shipped with a valid MAC address installed in flash in the protected ethaddr environmental variable of U-Boot. At boot time U-Boot automatically stores this address in a register within the MAC, which effectively provides it to any OS loaded after that point. Future releases of the SoM-9G20M will store the MAC address in the onboard serial flash.

4.3. Embedded Linux

EMAC Open Embedded Linux is an open source Linux distribution for use in embedded systems. The current SoM-9G20 build uses a Linux 2.6 kernel that has been has been patched to support the SoM-9G20 and SoM-150ES devices.

The distribution contains everything a user could expect from a standard Linux kernel, powerful networking features, advanced file system support, security, debugging utilities, and countless other features.

The SoM-9G20 will work out of the box with EMAC's Embedded Linux distribution, and EMAC provides the most up to date distribution via ftp. The SoM-9G20M comes preinstalled with a 2.6.20 or later Linux kernel.

4.3.1. Linux with Xenomai Real Time Extensions

Xenomai provides real time extensions to the kernel and can be used to schedule tasks with hard deadlines and μs latencies. The Xenomai build is an additional module that can be added to the standard Linux kernel and is available for a one-time inexpensive support/installation fee.

http://www.xenomai.org/

4.3.2. Linux Modules

EMAC provides support for many Linux modules such as: Cherokee Web Server, PHP, SQLite, Perl, SNMP, DHCP Server, etc. As with the Xenomai module, other modules can be added to the standard Linux filesystem and are available for a one-time inexpensive support/installation fee.

4.3.3. Linux 2.6 patches

In addition to standard Embedded Linux support, EMAC has released a number of patches and device drivers from the open source community and from internal EMAC engineering into its standard distribution. Currently, the kernel patches and some useful scripts may be downloaded from EMAC's SoM ftp site at:

ftp://ftp.emacinc.com/Controllers/SoM/SoM-9G20M/Software/Linux-Kernel/

Along with kernel patches, EMAC provides the binaries for the kernel and root file system.

4.4. Open Embedded

The Linux build for the SoM-9G20 is based on the Open Embedded (www.openembedded.org) Linux build system. The current kernel is Linux 2.6.20 or higher patched to support the SoM-9G20. Open Embedded is a superior Linux distribution for embedded systems. Custom Linux builds are also available on request.

The basic root filesystem includes:

- Busybox 1.9.2 or higher
- Hotplugging support
- APM utilities for power management
- Dropbear SSH server
- Telnet/FTP support running under inetd
- busybox-httpd HTTP server
- JFFS2 filesystem with utilities

4.5. ARM EABI Cross Compiler

The popular open source gcc compiler has a stable build for the ARM family. The Embedded Linux kernel and EMAC Eclipse CDT projects use this compiler for building ARM stand alone, and OS specific binaries. The EMAC Eclipse SDK provides source level debugging over either the JTAG port or over Ethernet or serial using gdbserver. The Linux binaries for the ARM EABI cross compiler are available online along with the SDK for the SoM-9G20 at the following location.

ftp://ftp.emacinc.com/Controllers/SoM/SoM-9G20M/Tools/

4.6. Windows CE 6.0

In addition to the open source community, a WinCE 6.0 BSP for the SoM-9G20 is under development and will be available soon.

4.7. Java

The AT91SAM9G20 includes the ARM Jazelle hardware which combined with the Jazelle software package provides an advanced multi-tasking Java Virtual Machine (JVM). The use of the Jazelle software requires a license from ARM and is not provided with the EMAC SDK. For more information see the following link.

http://www.arm.com/products/esd/jazelle_home.html

Note: All of the links in this document are subject to change. Please contact EMAC for updated link locations if necessary.

