SoM-200GS

User Manual

Revision 1.0

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1 Introduction

This document provides information regarding EMAC's SoM-200GS System on Module Carrier Board. The SoM-200GS is a versatile SoM Carrier board ideal for evaluation and early development work. This Carrier works with all EMAC 200-pin SODIMM type SoMs although not all functionality of a particular module may be supported.

The SoM-200GS provides access to virtually all of the 200-pin Module's I/O through on-board connectors as well as a number of additional I/O expansion blocks such as Digital I/O, Audio, and MMC/SD flash disk. Full schematics of the SoM-200GS are provided giving the user a solid base with which to design their own SoM Carrier.

Although a good deal of customers will want a Carrier that is unique and is designed specifically for their application, the SoM-200GS, when coupled with a SODIMM SoM makes for a powerful yet affordable Graphic User Interface (GUI) with USB and Ethernet capabilities. This allows the user to gather data and respond with Control commands via the Internet. An enclosure and power supply are available options for the SoM-200GS.

When a unique custom board is needed, the amount of design work required is greatly minimized by the SoM approach. The custom Carrier designer does not have to worry about the processor, memory, and standard I/O functions and can concentrate on the I/O and dimensional aspects required for the application.

In situations where a custom Carrier is required but the customer does not have the capability to design such a board in-house, EMAC's Custom to Order Services (COS) can be utilized. Using COS the customer can select from a library of standard I/O blocks. These blocks can be put together quickly into a form-factor of the customer's choosing, providing prototypes in as little as 30 days.

1.1 SoM Benefits

- Faster time to market
- Cost savings
- Reduced risk
- Scalable CPU choices
- Decreased customer design requirements
- Small footprint

1.2 Standard Features

(ports must also be supported by the SoM to provide functionality)

- **Small, Half EBX mounting hole form factor (4.375" x 6.00")**
- **10/100/1000 Base-T Ethernet with on-board Magnetics and RJ45**
- **3 serial RS232 ports and 1 RS232/422/485 port**
- **24 PLD controlled General Purpose digital I/O lines in addition to many SoM I/O lines**
  - **8 digital input lines**
  - **8 digital output lines**
  - **8 high drive digital output lines**
- **24 SoM based GPIOs**
- **Battery for nonvolatile RAM and Real Time Clock**
- **2 USB High Speed 2.0 Host ports (Dual Connector)**
- **1 USB High Speed Device port**
- **CAN 2.0 Port**
- **Audio:** I2S Audio Stereo CODEC
- **1 SPI Port and 1 I2C Port**
- **Micro SD Card Socket**
- **Power and MMC/SD card status LEDs**
- **Graphic LCD interface with WQVGA TFT LCD**
- **4-wire Resistive Touchscreen Interface**
- **System Reset button**
- **Optional Wi-Fi/BLE wireless** – 802.11 b/g/n & Bluetooth (W2CBW0015-T)

1.3 SoM-200GS Product Numbers

- **SOM-200GS-000** "Bare Bones" Version**:** 200-pin Carrier with SD Card (no PLD, Audio, Wifi, LCD)
- **SOM-200GS-001** "Standard" Version: 200-pin Carrier with SD Card, PLD, Audio and 4.3" LCD (no Wifi)
- **SOM-200GS-007** "Wi-Fi" Version: 200-pin Carrier with Wifi, Antenna kit, and 4.3" LCD (no SD Card)

1.4 Other Options

- **PER-ENC-00007:** This MicroBox metal chassis is an ideal housing for the SoM-200GS and Module.
- **PER-PWR-00041:** A 30 watt switching power supply that has an AC input of 100 to 240 volts and DC output of +5 / +12 volts.
- **PER-PWR-00032:** An inexpensive 13W AC/DC wall mount adapter that has an AC input of 110 volts, "US" DC output of +5 volts, and max output current of 2.5 Amps.
- **PER-PWR-00033:** An inexpensive 13W AC/DC wall mount adapter that has an AC input of 100 - 220 volts, "International" DC output of +5 volts, and max output current of 2.5 Amps.

2 Hardware

2.1 Specifications

- **VOLTAGE REQUIREMENTS:** 5 volt DC @ 2.0A board input voltage including SoM, USB and LCD. (Note: up to 1.0A of the 2.0A is required if USB Host is providing power to USB devices.)
- **CURRENT REQUIREMENTS:** ~800 mA @ 5 Volts Typical including SoM and LCD with no USB sourcing.
- **OPERATING TEMPERATURE:** 0°C - 60°C (-40°C - 85°C optional), humidity range without condensation 0% to 90% RH.
- **DIMENSIONS:** Half EBX mounting hole form factor with dimensions of 4.375" x 6.00".
- **DIGITAL I/O:** 8 digital input pins, 8 digital output pins with 20 mA drive, 8 open collector High-Drive Digital outputs with 500 mA sink drive capability, status LEDs, and a maximum total I/O drive of 1500 mA for these 8 lines. All Digital I/O lines terminate to standard 50 pin, I/O Rack compatible header connectors.
- **CAN TRANSCEIVER:** Non-Isolated CAN 3.3V Transceiver (TI SN65HVD230) terminating to a 10-pin header with terminating jumper. Includes 10-pin header to female DB9 connector cable.
- **OPTIONAL AUDIO INPUT/OUTPUT:** Line Level I2S Audio CODEC with Line-In and Line-Out standard Audio Jacks.

2.2 Jumpers

This section describes the Jumpers and Jumper Blocks of the SoM-200GS.

JB1
Boot Mode 0

The function of this jumper is determined by the SoM that is being utilized (see SoM user manual). This jumper is tied to SoM pin 157 (Boot Option 0). If the jumper is in the B position (default) then this line is pulled high. If the jumper is in the A position then the line is tied low.

JB2
Boot Mode 1

The function of this jumper is determined by the SoM that is being utilized (see SoM user manual). This jumper is tied to SoM pin 158 (Boot Option 1). If the jumper is in the B position then this line is tied high. If the jumper is in the A position (default) then the line is pulled low.

JB3
CAN Termination

Place a Jumper at position TRM to terminate CAN network. Place a Jumper at position OPN (default) to leave the termination resistor open.

JB4
Voltage Option

Place a jumper in the 5V position (default) to provide 5V to JB5. Place a jumper in the 12V position to route pin4 of HDR2 (normally 12V) to JB5. JB5 controls the pull-up voltage of the High Drive Output lines and determines what voltage is present on pin 49 of HDR3.

JB5

Pull-up Voltage Option JB5 controls the pull-up voltage of the High Drive Output lines and determines what voltage is present on pin 49 of HDR3. The left side of the jumper controls pin 49 and the right side controls the pull-up voltage of PortC. Leaving the left side shunt off leaves pin 49 open and leaving the right side shunt off sets the High Drive Outputs to no pull-up voltage. The voltage at the bottom two pins is defined by JB4.

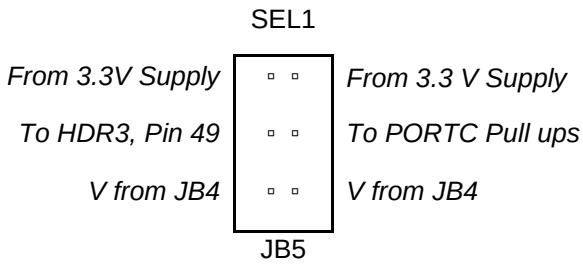

Figure 1: Typical shunt positions.

With both shunts in the lower position, the voltage selected by JB4 will be applied to pin 49 and Port C will be pulled up to that voltage. With both shunts in the upper position, 3.3V will be applied to pin 49 and Port C will be pulled up to 3.3V.

JB6

Battery Saver Jumper Position JB6 to “ON” to provide Battery Backup of RTC. Position to “OFF” (default) to preserver battery while in storage.

JB7

Flash Write Protect Position JB7 to the A position to provide to write protect protection for SoM resident flash. Position to the B position (default), to allow writes to flash.

JB8

Ethernet Primary Tap Position JB8 to “OPN” to provide gigabit Ethernet capabilities. Position JB8 to “3P3” to provide 10/100 Base-T Ethernet capabilities of the SoM.

JB9

422/485 Place a Jumper at position TRM to terminate the Rx pair with a 120Ω resistor, while operating in 422/485 mode. Place a Jumper at position OPN (default) to leave the termination resistor open, while operating in 232 mode.

2.3 JTAG Header

This multipurpose header provides an in-circuit programming interface to the Max II CPLD that resides on the SoM-200GS as well as any PLD or debug port on the SoM itself. This header can be used to reprogram the onboard CPLD and any other CPLDs detected on the JTAG chain (on the module). This 14 pin connector (HDR9) provides a standard JTAG connection meant to connect directly to a JTAG Debugger supporting this standard. EMAC also provides an adapter board (PER-ADP-00020), which makes the Carrier's PLD JTAG come out to a standard 10-pin header and also provides the alternate 20 pin JTAG connector for the module.

This requires an interface cable, such as the ByteBlasterMV. Several models are available from Altera. Also more inexpensive versions and open schematics can be obtained via the Internet.

Table 1: JTAG Header (HDR9)

Pin	Signal	Pin	Signal
1	3.3Vdc	2	GND
3	JTAG_TRST	4	GND
5	JTAG_TDI	6	PLD_JTAG_TDI
7	JTAG_TMS	8	PLD_JTAG_TMS
9	JTAG_TCK	10	PLD_JTAG_TCK
11	JTAG_TDO	12	NC
13	JTAG_RTCK	14	PLD_JTAG_TDO

2.4 Module Based I/O

The Module I/O connector, HDR1 is made up primarily of direct connections from the modules SODIMM connector. The only signals that do not directly come from the module are the power supply signals and PLD signals: GPIO4, GPIO5, GPIO6, GPIO18, and GPIO19.

Table 2: SoM I/O Connector (HDR1)

Pin	DESCRIPTION	Pin	DESCRIPTION
1	SPI_MISO	2	RESET_OUT
3	SPI_MOSI	4	GND
5	SPI_SCLK	6	GPIO17
7	SPI_CS0	8	GND
9	SPI_CS1	10	ANALOG_04
11	SPI_CS3	12	ANALOG_05
13	GPIO16	14	ANALOG_06
15	GPIO1	16	ANALOG_07
17	GPIO2	18	GND
19	GPIO3	20	GND
21	GPIO4	22	GPIO18
23	GPIO5	24	GPIO19
25	GPIO6	26	GND
27	GPIO7	28	GND
29	GPIO12	30	GND
31	GPIO13	32	GND
33	GPIO15	34	GND
35	I2C_CLK	36	GND
37	I2C_DATA	38	GND
39	INT0	40	GND
41	INT1	42	GND
43	GPIO14	44	GND
45	CLK_Fast	46	GND
47	CLK_Slow	48	GND
49	3.3V DC	50	GND

2.5 CPLD Based General Purpose Digital I/O

The SoM-200GS provides 24 general-purpose 3.3V I/O pins connected to header HDR3. These pins are controlled by an Altera Max II device, which is an in-circuit programmable, instant on, CPLD. By default this is the EPM240T100C5 model, which provides 150 internal logic elements, but it is pin-compatible with some larger devices. This CPLD provides powerful reconfigurable combinational and sequential logic, for an almost unlimited number of applications. Through Altera's free Quartus II environment, this device can be easily reconfigured as digital I/O, counters, UARTs, SPI, even flash and RAM. The CPLD interfaces through the address and data bus of the carrier, and has access to clocks and an IRQ for advanced control logic. When the SoM-200GS is produced, the PLD is pre-loaded with a configuration that it instantly loads upon power-up. This configuration uses the pins in a specific manner, which is described in the rest of this section, but could be easily reprogrammed to be something else. EMAC provides free drivers and development software for interfacing with the standard configuration.

The default program creates 3 digital ports, Ports A, B, and C. Port A and Port B are independently bit programmable outputs or inputs. When programmed as inputs the input lines should not exceed 3.3V DC. If programmed as outputs, these lines are capable of driving 25 mA loads. The open collector high drive output Port C (PC0 – PC7) has a 500 mA sink drive capability and a maximum total I/O drive of 1500 mA. The PLD has input capabilities on these 8 lines for modularity reasons, but they are not useable as such in the actual system. The voltage on pin 49 as well as the pull-up voltage for Port C is controlled by jumpers JB4 and JB5. See the Jumper section for additional details.

Table 3: CPLD Based Digital I/O Connector (HDR3)

Pin	Signal	Pin	Signal
1	PA0 (3.3V)	2	GND
3	PA1 (3.3V)	4	GND
5	PA2 (3.3V)	6	GND
7	PA3 (3.3V)	8	GND
9	PA4 (3.3V)	10	GND
11	PA5 (3.3V)	12	GND
13	PA6 (3.3V)	14	GND
15	PA7 (3.3V)	16	GND
17	PB0 (3.3V)	18	GND
19	PB1 (3.3V)	20	GND
21	PB2 (3.3V)	22	GND
23	PB3 (3.3V)	24	GND
25	PB4 (3.3V)	26	GND
27	PB5 (3.3V)	28	GND
29	PB6 (3.3V)	30	GND
31	PB7 (3.3V)	32	GND
33	PC0 (High Drive)	34	GND
35	PC1 (High Drive)	36	GND
37	PC2 (High Drive)	38	GND
39	PC3 (High Drive)	40	GND
41	PC4 (High Drive)	42	GND
43	PC5 (High Drive)	44	GND
45	PC6 (High Drive)	46	GND
47	PC7 (High Drive)	48	GND
49	3.3/5/Vin	50	GND

2.5.1 Memory Map

The SoM-200GS's PLD is connected to the SoM's processor data bus and has the ability to use the SODIMM pins 145, 146, 147, and 148 as chip select lines. GP_CSB (SODIMM pin 146) is used as the default chip select for the memory map. The base addresses of the chip selects used by the PLD are SoM dependent.

For additional information go to:

http://wiki.emacinc.com/wiki/Using_the_EMAC_GPIO_Class

Within the PLD are several registers that are referenced as offsets from the PLD Base address. They are defined as follows:

Table 4: Default CPLD Memory Map

Offset	Register	Description
0	PortA Data	Digital State
1	PortA Configuration	Input/Output Mapping
2	PortB Data	Digital State
3	PortB Configuration	Input/Output Mapping
4	PortC Data	Digital State
5	PortC Configuration	Input/Output Mapping
6	RS-232/422/485 Control	Output
15	CPLD Key	Input

2.5.2 Register Descriptions

Port Data Registers

The bits of these ports are mapped to the data lines of the physical ports. Writing to these bits latches the 3.3V DC Vcc or GND value (one or zero respectively) to the appropriate pin. Pins are mapped according to their respective positions on the header, i.e. PB4 has its value latched by the 4th bit of the Port B configuration register.

Latching a bit will result in a voltage change at the pin if the pin is configured to be an output with the corresponding configuration register bit. Reading from this address will return the current state (one or zero for Vcc or GND) of the pin.

Port Configuration Registers

This port is bitwise mapped to the configuration of the ports. Setting a bit to 1 sets the corresponding pin to an output. Setting a bit to 0, sets it as an input. For example: Setting the Port B configuration register to 0x10 would set PB4 to be an output and place its current latched state (see the Data Register description) on the pin.

2.5.3 Other CPLD Functions

The CPLD also provides Serial Port enable/disable/shutdown control for serial ports: A, B and D. There are unused interrupt and chip select lines connected to the PLD allowing for feature enhancements.

2.6 Serial Ports

2.6.1 RS 232 Serial COMA

The SoM-200GS provides one dedicated RS232 serial port accessible via a male DTE DB9 connector that has a full complement of handshaking signals. Note: the baud rate and the actual number of handshaking signals are determined by the SoM being used. Refer to the SoM manual for this information.

Table 5: Serial Port COMA (CN1)

Pin	Pin Description for DB9 Connector
1	DCD_IN
2	RxD_IN
3	TxD_OUT
4	DTR_OUT
5	GND
6	DSR_IN
7	RTS_OUT
8	CTS_IN
9	RI_IN

2.6.2 RS 232 Serial COMB

Serial UART COMB is a dedicated RS232 serial port accessible via a 10-pin header (HDR4) connector with two handshaking signals. EMAC provides a male DB9 DTE serial cable that plugs into this header and provides a standard serial interface.

Note: the baud rate and the handshaking signals are determined by the SoM being used. Refer to the SoM manual for this information. The pin-out of the header and the DB9 are as follows:

Table 6: Serial Port COMB (HDR4)

Pin	Pin Description for 10-Pin Header	Pin Description for DB9 Connector
1	NC	NC
2	NC	RxD_IN
3	RxD_IN	TxD_OUT
4	RTS_OUT	NC
5	TxD_OUT	GND
6	CTS_IN	NC
7	NC	RTS_OUT
8	NC	CTS_IN
9	GND	NC
10	NC	-

2.6.3 RS 232/422/485 Serial COMC

The SoM-200GS provides one muti-mode serial port. This port is software configurable as RS232, RS422, or RS485, with the default being “off”. When used as an RS232 port, two handshake lines are provided, CTS and RTS. Switching from RS232 to RS422 or RS485 is controlled by four processor based SoM socket signals.

The Tables below describe the state of the control signals for the various serial port modes. For more information on serial ports and software configuration go to:

http://wiki.emacinc.com/wiki/Example_serport212

Table 7: Serial Port COMC RS232 (default) Mode

Signal	**SODIMM Pin#**	**State**
GPIO6	120	Low
GPIO4	118	High
GPIO5	119	High

Table 8: Serial Port COMC RS422 Mode

Signal	**SODIMM Pin#**	**State**
GPIO6	120	High
GPIO4	118	Low
GPIO5	119	Low

Table 9: Serial Port COMC RS485 Transmit Mode

Signal	**SODIMM Pin#**	**State**
GPIO6	120	High
GPIO4	118	Low
GPIO5	119	Low
COMC_RTS	109	High

Table 10: Serial Port COMC RS485 Receive Mode

Signal	**SODIMM Pin#**	**State**
GPIO6	120	High
GPIO4	118	Low
GPIO5	119	Low
COMC_RTS	109	Low

The connections to serial port COMC are made through a 10-pin header (HDR5). EMAC provides a male DB9 DTE serial cable that plugs into this header and provides a standard interface. Note: when wiring for RS485 mode short TX+ and RX+ and short TX- and RX- together. The pin-out of the header and the DB9 are as follows:

Table 11: Serial Port COMC (HDR5)

Pin	**Pin Description for 10-Pin Header**	**Pin Description for DB9 Connector**
1	232 DCD, 422/485 TX-	232 DCD, 422/485 TX-
2	NC	232 RX, 422/485 TX+
3	232 RX, 422/485 TX+	232 TX, 422/485 RX+
4	RTS	232 DTR, 422/485 RX-
5	232 TX, 422/485 RX+	GND
6	CTS	NC
7	232 DTR, 422/485 RX-	RTS
8	NC	CTS
9	GND	NC
10	NC	-

2.6.4 RS 232 Serial UART COMD

Serial UART COMD is a dedicated RS232 serial port accessible via a 10-pin header (HDR6) connector with two handshaking signals. EMAC provides a male DB9 DTE serial cable that plugs into this header and provides a standard interface. Note: the baud rate and the handshaking signals are determined by the SoM being used. Refer to the SoM manual for this information. The pinout of the header and the DB9 are as follows:

Table 12: Serial Port COMD (HDR6)

Pin	Pin Description for 10-Pin Header	Pin Description for DB9 Connector
1	NC	NC
2	NC	RxD_IN
3	RxD_IN	TxD_OUT
4	RTS_OUT	NC
5	TxD_OUT	GND
6	CTS_IN	NC
7	NC	RTS_OUT
8	NC	CTS_IN
9	GND	NC
10	NC	-

2.7 CAN Port

The SoM-200GS provides a CAN 2.0 port utilizing the TI SN65HVD232 CAN Transceiver chip. Note the CAN controller must be supported by the SOM in order to have CAN functionality The CAN port is accessible via a 10-pin header (HDR7). EMAC provides a male DB9 DTE serial cable that plugs into this header and provides a standard interface. The pinout of the header and the DB9 are as follows:

Table 13: CAN Port CAN (HDR7)

Pin	Pin Description for 10-Pin Header	Pin Description for DB9 Connector
1	NC	NC
2	NC	CAN_LOW
3	CAN_LOW	GND
4	CAN_HIGH	NC
5	GND	GND
6	NC	NC
7	NC	CAN_HIGH
8	NC	NC
9	GND	NC
10	NC	-

2.8 Audio

The SoM-200GS optionally provides an I2S Stereo CODEC with standard line level input and output jacks. The CODEC used on the SoM-200GS is the Cirrus Logic CS4271. Jack JK4 is the audio input and JK5 is the audio output. Volume and Balance are controlled through software using the SPI bus with SPI_CS2. Note: I2S audio must be supported by the SoM for the audio port to function.

2.9 LCD

The LCD interface provides a specific LCD connector (SOK3) and backlight driver for the Fema GM480272X WQVGA LCD. This LCD can be mounted directly to the SoM-200 PCB board using a special bracket provided by EMAC. The SoM-200GS also provides a generic connector (HDR8) for connecting to other LCDs. The backlighting can be controlled via software via the SoM Backlight signal (SoM pin 85). The LCD can be turned on and off via the SoM GPIO0 signal (pin 114).

Table 14: LG LCD Interface (SOK3)

Pin	Signal
FN2	GND
40	TCHSCR Y2- [TE]
39	TCHSCR X2- [LE]
38	TCHSCR Y1+ [BE]
37	TCHSCR X1+ [RE]
36	GND
35	NC
34	DATA ENABLE
33	NC
32	NC
31	DISP ON/OFF
30	CLK
29	GND
28	BLUE DAT 7 (MSB)
27	BLUE DAT 6
26	BLUE DAT 5
25	BLUE DAT 4
24	BLUE DAT 3
23	BLUE DAT 2
22	BLUE DAT 1
21	BLUE DAT 0 (LSB)
20	GRN DAT 7 (MSB)
19	GRN DAT 6
18	GRN DAT 5
17	GRN DAT 4
16	GRN DAT 3
15	GRN DAT 2
14	GRN DAT 1
13	GRN DAT 0 (LSB)
12	RED DAT 7 (MSB)
11	RED DAT 6
10	RED DAT 5
9	RED DAT 4
8	RED DAT 3
7	RED DAT 2
6	RED DAT 1
5	RED DAT 0 (LSB)
4	VCC
3	GND
2	LED+
1	LED-
FN1	GND

Table 15: Alternate LCD Interface (HDR8)

Pin	Signal	Pin	Signal
1	5V_VCC	2	5V_VCC
3	+12_ACCY	4	+12_ACCY
5	3.3V	6	3.3V
7	GND	8	GND
9	BLUE0	10	BLUE1
11	BLUE2	12	BLUE3
13	BLUE4	14	BLUE5
15	BLUE6	16	BLUE7
17	GREEN0	18	GREEN1
19	GREEN2	20	GREEN3
21	GREEN4	22	GREEN5
23	GREEN6	24	GREEN7
25	RED0	26	RED1
27	RED2	28	RED3
29	RED4	30	RED5
31	RED6	32	RED7
33	GND	34	GND
35	LCD_CLK	36	VSYNC
37	LCD_EN	38	HSYNC
39	BACKLIGHT	40	GPIO0/DISP_ON/OFF
41	TOUCHF_X+	42	TOUCHF_X-
43	TOUCHF_Y+	44	TOUCHF_Y-

2.10 Ethernet

The SoM-200GS provides the magnetics and RJ45 connector for a standard 10/100/1000 Base-T port. Additionally two LEDs are provided for Activity and Link status. The RJ45 is pinned as a standard 10/100/1000 Base-T Ethernet port and thus should work with any standard router or switch. Note: If using the SoM-200GS with a SoM that does not support 1000 BaseT, jumper JB8 must be jumpered (see jumper section of this manual).

2.11 USB

The SoM-200GS provides for dual USB host ports (USB PortA & PortB). The USB host ports are fused with automatically resettable Polyfuses. If a USB device tries to draw more than 500 milliamps, the fuses will open. Once the drawing source is removed the fuses will automatically reset. The USB ports are pinned as standard USB host ports and thus should work with any standard USB mating device or host.

In addition to the two USB Host ports is a USB OTG Host/Device port. This port can be used as either a USB Host or USB Device port and is also fused when used as a Host (functionality of this port is determined by the SoM).

Note: When sizing a power supply, make sure to allow for USB Device consumption. A device can potentially draw 500mA, therefore these devices could use a total of up to 1.5 amp of power. USB ports must be supported by the SoM for the ports to operate.

2.12 Multi-media (MMC) / Secure Digital (SD) Card Socket

The SoM-200GS provides a micro SD/MMC type socket, which accepts SD and MMC cards. This Socket is connected to the processor's SDIO. A SD/MMC activity LED is available on GPIO8 (SoM pin 122). The voltage supply to the SD/MMC socket can be shut down using GPIO9/SD_PWREN (SoM pin 123). The only signal that does not directly come from the SODIMM socket is the power supply signal VCC. Note: the SD Card socket is not available with the Wifi option.

Table 16: SD/MMC Socket (SOK2)

Pin	Parallel Mode Signal	SoM Signal	SODIMM Pin
1	DAT2	DAT2	35
2	CD/DAT3	DAT3	36
3	CMD	CMD	32
4	VDD	VCC	-
5	CLK	SCLK	31
6	VSS	GND	-
7	DAT0	DAT0	33
8	DAT1	DAT1	34
9	SW_A	Card_Detect	37
10	SW_B	GND	-

2.13 Wi-Fi [optional]

The SoM-200GS provides a Wi-Fi/Bluetooth antenna jack (JK7) connected to the on-board Wi-Fi/ 802.11 module. The antenna jack, (U.FL-R-SMT(10)) offers high frequency performance from DC to 6GHz, with a V.S.W.R of 1.3 to 1.5 max. EMAC provides an antenna kit included with the Wi-Fi option: 2.4GHz Duck Antenna RP-SMA and U.FL.(IPEX) to RP-SMA male pigtail cable that plugs into the SoM's antenna jack. The Wi-Fi/ 802.11 module is a complete wireless subsystem featuring full 802.11 b/g/n WLAN + BT capabilities in a small form factor module solution. The Wi-Fi module exclusively trades places with the legacy SD card interface by population option. Due to SD Bus limitations both cannot be present and useable on the same board. The table below lists the data and control signals provided by the 200-pin SODIMM socket.

Table 17: Wi-Fi

Parallel Mode Signal	*SoM Signal*	SODIMM Pin
PD	GPIO10	124
RESET	GPIO9	123
SD_CLK/SPCK	SCLK	31
SD_CMD/MISO	CMD	32
SD_D0/MOSI	DAT0	33
SD_D1/IRQ	DAT1	34
SD_D2/RESV	DAT2	35
SD_D3/SPCS	DAT3	36

3 Software

The SoM-200GS is programmable via a selection of free software tools and open source EMAC software. Software Board Support Packages (BSPs) and Linux Software Development Kits (SDKs) are available for most SoM processor modules.

3.1 Introduction

Whichever module is used in the SOM-200GS can be programmed in a variety of languages and utilize a variety of Operating Systems. There are a number of free compilers, interpreters, and assemblers available allowing the processor Module to be programmed in C, BASIC, or Assembly languages. EMAC has Board Support Packages available for Linux. For more information on these particular Operating Systems, contact EMAC, Inc.

For more information on Linux Software Support, please visit the EMAC Wiki Software Section at:

http://wiki.emacinc.com/wiki/product_wiki

3.2 U-Boot

EMAC utilizes Das U-Boot for its ARM based products. U-Boot is an open source/cross-architecture platform independent bootloader. It supports reading and writing to the flash, auto-booting, environmental variables, and TFTP. Das U-boot can be used to upload and run and/or reflash the OS or to run stand-alone programs without an OS. Products are shipped with a valid MAC address installed in flash in the protected U-boot environmental variable “ethaddr”. At boot time U-Boot automatically stores this address in a register within the MAC, which effectively provides it to any OS loaded after that point.

3.3 Embedded Linux

EMAC Open Embedded Linux is an open source Linux distribution for use in embedded systems. The EMAC OE Linux Build is based on the Open Embedded (www.openembedded.org) Linux build system. Open Embedded is a superior Linux distribution for embedded systems. Custom Linux builds are also available on request.

The distribution contains everything a user could expect from a standard Linux kernel: powerful networking features, advanced file system support, security, debugging utilities, and countless other features.

The basic root file system includes:

- Busybox
- Hotplugging support
- APM utilities for power management
- Openssh SSH server
- lighttpd HTTP server
- JJFS2 or EXT4 file system with utilities

3.3.1 Linux with Xenomai Real Time Extensions

Xenomai provides real time extensions to the kernel and can be used to schedule tasks with hard deadlines and μs latencies. The Xenomai build is an additional module that can be added to the standard Linux kernel and is available for a one-time inexpensive support/installation fee.

http://www.xenomai.org/

3.3.2 Linux Packages

EMAC provides support for many Linux Packages such as: PHP, SQLite, Perl, SNMP, DHCP Server, etc. As with the Xenomai Package, other Packages can be added to the standard Linux file system and are available for a one-time inexpensive support/installation fee.

3.3.3 Linux Patches

In addition to standard Embedded Linux support, EMAC has released a number of patches and device drivers from the open source community and from internal EMAC engineering into its standard distribution. Along with kernel patches, EMAC provides the binaries for the kernel and root file system.

3.4 Qt Creator

Qt Creator is a cross-platform IDE (Integrated Development Environment) tailored to the needs of Qt developers but works well for Headless applications as well. EMAC provides sample code as projects that can be imported into Qt Creator. Qt Creator supports remote deployment and source debugging.

https://qt-project.org/wiki/Category:Tools::QtCreator

3.5 ARM EABI Cross Compiler

The popular open source gcc compiler has a stable build for the ARM family. EMAC uses the 4.9.1 version of the ARM EABI compiler. The Embedded Linux kernel and EMAC Qt Creator projects use this compiler for building ARM stand alone, and OS specific binaries. The EMAC Qt Creator provides source level debugging over Ethernet or serial using gdbserver. The Linux binaries for the ARM EABI cross compiler are available online along with the SDK. See the EMAC wiki for further information.

3.6 Quartus II Web Edition

Altera offers powerful free tools for programming the Max II plus PLD of the SoM-200GS. These tools include free and flexible modules for implementing UARTs, I2C, counters, RAM, Flash, etc.

https://www.altera.com/support/software/download/altera_design/quartus_we/dnl-quartus_we.jsp

4 Appendix A: Connector Pinouts

4.1 SoM I/O Connector (HDR1)

Pin	DESCRIPTION	Pin	DESCRIPTION
1	SPI_MISO	2	RESET_OUT
3	SPI_MOSI	4	GND
5	SPI_SCLK	6	GPIO17
7	SPI_CS0	8	GND
9	SPI_CS1	10	ANALOG_04
11	SPI_CS3	12	ANALOG_05
13	GPIO16	14	ANALOG_06
15	GPIO1	16	ANALOG_07
17	GPIO2	18	GND
19	GPIO3	20	GND
21	GPIO4	22	GPIO18
23	GPIO5	24	GPIO19
25	GPIO6	26	GND
27	GPIO7	28	GND
29	GPIO12	30	GND
31	GPIO13	32	GND
33	GPIO15	34	GND
35	I2C_CLK	36	GND
37	I2C_DATA	38	GND
39	INT0	40	GND
41	INT1	42	GND
43	GPIO14	44	GND
45	CLK_Fast	46	GND
47	CLK_Slow	48	GND
49	3.3V DC	50	GND

4.2 Drive Power Connector Input (HDR2)

Pin	Signal
1	+5V
2	GND
3	GND
4	+12V (Vin)

4.3 Power Jack (JK6)

Pin	Signal
Center	5V DC
Barrel	GND

4.4 Ethernet (JK1)

Pin	Signal
1	MX1+
2	MX1-
3	MX2+
4	MX3+
5	MX3-
6	MX2-
7	MX4+
8	MX4-

4.5 PLD Based Digital I/O Connector (HDR3)

Pin	Signal	Pin	Signal
1	PA0 (3.3V)	2	GND
3	PA1 (3.3V)	4	GND
5	PA2 (3.3V)	6	GND
7	PA3 (3.3V)	8	GND
9	PA4 (3.3V)	10	GND
11	PA5 (3.3V)	12	GND
13	PA6 (3.3V)	14	GND
15	PA7 (3.3V)	16	GND
17	PB0 (3.3V)	18	GND
19	PB1 (3.3V)	20	GND
21	PB2 (3.3V)	22	GND
23	PB3 (3.3V)	24	GND
25	PB4 (3.3V)	26	GND
27	PB5 (3.3V)	28	GND
29	PB6 (3.3V)	30	GND
31	PB7 (3.3V)	32	GND
33	PC0 (High Drive)	34	GND
35	PC1 (High Drive)	36	GND
37	PC2 (High Drive)	38	GND
39	PC3 (High Drive)	40	GND
41	PC4 (High Drive)	42	GND
43	PC5 (High Drive)	44	GND
45	PC6 (High Drive)	46	GND
47	PC7 (High Drive)	48	GND
49	3.3V/5V/Vin	50	GND

4.6 Serial Port COMA (CN1)

Pin	Pin Description for DB9 Connector
1	DCD_IN
2	RxD_IN
3	TxD_OUT
4	DTR_OUT
5	GND
6	DSR_IN
7	RTS_OUT
8	CTS_IN
9	RI_IN

4.7 Serial Port COMB (HDR4)

Pin	Pin Description for 10-Pin Header	Pin Description for DB9 Connector
1	NC	NC
2	NC	RxD_IN
3	RxD_IN	TxD_OUT
4	RTS_OUT	NC
5	TxD_OUT	GND
6	CTS_IN	NC
7	NC	RTS_OUT
8	NC	CTS_IN
9	GND	NC
10	NC	-

4.8 Serial Port COMC (HDR5)

Pin	Pin Description for 10-Pin Header	Pin Description for DB9 Connector
1	232 DCD, 422/485 TX-	232 DCD, 422/485 TX-
2	NC	232 RX, 422/485 TX+
3	232 RX, 422/485 TX+	232 TX, 422/485 RX+
4	RTS	232 DTR, 422/485 RX-
5	232 TX, 422/485 RX+	GND
6	CTS	NC
7	232 DTR, 422/485 RX-	RTS
8	NC	CTS
9	GND	NC
10	NC	-

4.9 Serial Port COMD (HDR6)

Pin	Pin Description for 10-Pin Header	Pin Description for DB9 Connector
1	NC	NC
2	NC	RxD_IN
3	RxD_IN	TxD_OUT
4	RTS_OUT	NC
5	TxD_OUT	GND
6	CTS_IN	NC
7	NC	RTS_OUT
8	NC	CTS_IN
9	GND	NC
10	NC	-

4.10 Module SODIMM Connector (SOK1)

(see 200-Pin SoM Pin Specification and Reference Schematics)

4.11 SD/MMC Socket (SOK2)

Pin	Parallel Mode Signal	SoM Signal	SODIMM Pin
1	DAT2	DAT2	35
2	CD/DAT3	DAT3	36
3	CMD	CMD	32
4	VDD	VCC	-
5	CLK	SCLK	31
6	VSS	GND	-
7	DAT0	DAT0	33
8	DAT1	DAT1	34
9	SW_A	Card_Detect	37
10	SW_B	GND	-

4.12 CAN Termination (HDR7)

Pin	Signal	Pin	Signal
1	NC	2	NC
3	CANL	4	CANH
5	GND	6	NC
7	NC	8	NC
9	GND	10	NC

4.13 USB PortA (JK2 Bottom – HostA)

Pin	Signal
1	USB_PWR (5V DC)
2	USB_Data-
3	USB_Data+
4	GND

4.14 USB PortB (JK2 Top – HostB)

Pin	Signal
1	USB_PWR (5V DC)
2	USB_Data-
3	USB_Data+
4	GND

4.15 USB OTG PortC (JK3)

Pin	Signal
1	USB_OTG_VBUS
2	USB_OTG_Data-
3	USB_OTG_Data+
4	USB_OTG_ID
5	GND
6	SHLD
7	SHLD

4.16 Alternate LCD Interface (HDR8)

Pin	Signal	Pin	Signal
1	5V_VCC	2	5V_VCC
3	+12_ACCY	4	+12_ACCY
5	3.3V	6	3.3V
7	GND	8	GND
9	BLUE0	10	BLUE1
11	BLUE2	12	BLUE3
13	BLUE4	14	BLUE5
15	BLUE6	16	BLUE7
17	GREEN0	18	GREEN1
19	GREEN2	20	GREEN3
21	GREEN4	22	GREEN5
23	GREEN6	24	GREEN7
25	RED0	26	RED1
27	RED2	28	RED3
29	RED4	30	RED5
31	RED6	32	RED7
33	GND	34	GND
35	LCD_CLK	36	VSYNC
37	LCD_EN	38	HSYNC
39	BACKLIGHT	40	GPIO0|DISP_ON/OFF
41	TOUCHF_X+	42	TOUCHF_X-
43	TOUCHF_Y+	44	TOUCHF_Y-

4.17 LG LCD Interface (SOK3)

Pin	Signal
FN2	GND
40	TCHSCR Y2- [TE]
39	TCHSCR X2- [LE]
38	TCHSCR Y1+ [BE]
37	TCHSCR X1+ [RE]
36	GND
35	NC
34	DATA ENABLE
33	NC
32	NC
31	DISP ON/OFF
30	CLK
29	GND
28	BLUE DAT 7 (MSB)
27	BLUE DAT 6
26	BLUE DAT 5
25	BLUE DAT 4
24	BLUE DAT 3
23	BLUE DAT 2
22	BLUE DAT 1
21	BLUE DAT 0 (LSB)
20	GRN DAT 7 (MSB)
19	GRN DAT 6
18	GRN DAT 5
17	GRN DAT 4
16	GRN DAT 3
15	GRN DAT 2
14	GRN DAT 1
13	GRN DAT 0 (LSB)
12	RED DAT 7 (MSB)
11	RED DAT 6
10	RED DAT 5
9	RED DAT 4
8	RED DAT 3
7	RED DAT 2
6	RED DAT 1
5	RED DAT 0 (LSB)
4	VCC (3.3V)
3	GND
2	LED+
1	LED-
FN1	GND

4.18 JTAG Header (HDR9)

Pin	Signal	Pin	Signal
1	3.3VDC	2	GND
3	JTAG_TRST	4	GND
5	JTAG_TDI	6	PLD JTAG TDI
7	JTAG_TMS	8	PLD JTAG TMS
9	JTAG_TCK	10	PLD JTAG TCK
11	JTAG_TDO	12	NC
13	JTAG_RTCK	14	PLD JTAG TD

5 Appendix B: Jumper Settings

(See SoM Module manual for correct Boot jumper settings)

JB1 Boot Mode 0 Selection

Jumper	Position	Setting
Pins 2 & 3	A	Line pulled LOW
Pins 1 & 2*	B	Line pulled HIGH

* Default setting

JB2 Boot Mode 1 Selection

Jumper	Position	Setting
Pins 2 & 3*	A	Line pulled LOW
Pins 1 & 2	B	Line pulled HIGH

* Default Setting

JB3 CAN Termination

Jumper	Position	Setting
Pins 1 & 2	TRM	Terminates CAN Network
Pins 2 & 3*	OPN	Leaves resistor open

* Default setting

JB4 Voltage Option

Jumper	Position	Setting
Pins 1 & 2	12V	12v to JB5
Pins 2 & 3*	5V	5V to JB5

* Default setting

JB5 Pull-up Voltage Option

Jumper	Position	Setting
Pins 1 & 3, 2 & 4*	Both Upper	3.3V to Pin49 and PORTC
Pins 3 & 5, 4 & 6	Both Lower	JB4 voltage to Pin49 and PORTC

* Default setting

JB6 Battery Saver

Jumper	Position	Setting
Pins 1 & 2	ON	Battery Backup
Pins 2 & 3*	OFF	Preserves Battery

* Default setting

JB7 FLASH Write Protect

Jumper	Position	Setting
Pins 2 & 3	A	Write Protection
Pins 1 & 2*	B	Write to FLASH

* Default setting

JB8 Ethernet Primary Tap

Jumper	Position	Setting
Pins 2 & 3	3P3	10/100 BaseT Ethernet
Pins 1 & 2*	OPN	10/100/1000 BaseT Ethernet

* Default setting

JB9 422/485

Jumper	Position	Setting
Pins 2 & 3*	OPN	232 mode
Pins 1 & 2	TRM	422/485 mode

* Default setting

6 Appendix C: Mechanical Drawing with Dimensions