

PCM-1812 MANUAL

104-1812CLD2N

Embedded 104 Single Board
Computer

Version: A0

Announcement

The information in this manual represents no promise or guarantee by the manufacturer.

The manufacturer reserves the right to make changes to the manual, without prior notice to customer. The manufacturer will not be held liable for any direct, indirect, intended or unintended losses and/or hidden dangers due to installation or improper operation.

Safety Instructions

1. Please read the *User Guide* carefully before using the product;
2. Please keep the motherboard in the static-shielding bag before inserting;
3. Before taking the motherboard out of the static-shielding bag, please touch with metal objects for a while (e.g. 10 seconds) to release the static on the hand;
4. Wear anti-static glove before handling the motherboard and always hold a board by its edges;
5. Before inserting, removing or re-configuring motherboard or expansion card, first disconnect the computer and peripherals from their power sources;
6. Before removing boards or computer, first turn off all power resources and disconnect the power cord from power source;
7. For PC Box products, when inserting or removing boards, first disconnect the computer and peripherals from their power sources;
8. Before connecting or unplugging any signal cable, make sure all power cords are unplugged in advance;
9. To avoid unnecessary damage caused by turning on/off computer frequently, wait at least 30 seconds before re-turning on the computer.

Contents

Chapter 1 Product Introduction	1
Overview	1
Environment and Mechanical Dimension	1
Typical Power Consumption	1
CPU	2
Chipset	2
System Memory	2
Video Function	2
Network Function	2
Power Features	2
Expansion Bus	3
IDE Function	3
I/O Function	3
Watchdog Function	3
Chapter 2 Installation	4
Product Dimension Drawing	4
Locations of Interfaces	5
Jumper Function Setup	6
LCD Backlight Controlling	7
SATA Interface	7
IDE Interface	8
USB Interface	8

Video Interface	9
Multi-function Interface	9
LAN Port	10
Digital I/O Interface.....	10
Power Interface.....	11
Fan Interface	11
Serial Port	11
CF Card.....	12
PC104 Interface.....	13
Chapter 3 BIOS Setup	14
Description for Display Driver	14
Appendix.....	15
Watchdog Programming Guide.....	15
GPIO Programming Guide.....	18
I/O Address Map.....	20
IRQ Assignment Table	21

Chapter 1 Product Introduction

Overview

This is an industrial embedded PC104 motherboard with high performance, low consumption. It adopts Intel Atom N270 processor and Mobile Intel 945GSE + ICH7-M chipset, the maximum power consumption of the motherboard is controlled below 12W (include CF card, 1G on-board memory); it is fan-less, stable, safe, reliable and can adapt wide-temperature environment (the originally supported operating temperature is $-40^{\circ}\text{C} \sim +80^{\circ}\text{C}$), has high practicability, etc. This product can be widely used in the fields of war industry, medical treatment, numerical controlling and traffic, etc.

Environment and Mechanical Dimension

- Operating Environment
Temperature: $-40^{\circ}\text{C} \sim +80^{\circ}\text{C}$;
Humidity: 5%~90% (Non-condensing);
- Storage Environment
Temperature: $-45^{\circ}\text{C} \sim +85^{\circ}\text{C}$;
Humidity: 5%~90% (Non-condensing);
- Dimension: 115.62mm x 97.00mm.

Typical Power Consumption

CPU: On-board Intel Atom 1.6G

Memory: On-board 1G DDR2 533MHz

- +5V@2.24A; +5%/-3%;

CPU

Intel Atom N270 1.6G/533MHz/512k/FCBGA8-437 CPU.

Chipset

Intel QG82945GSE+ NH82801GBM (ICH7M).

System Memory

On-board 1G Memory (DDR2/533MHz).

Video Function

This board adopts Mobile Intel 945GSE chipset, integrates video module, and can assign display memory according to requirements. It also supports VGA, dual-channel LVDS display (18 bit) and VGA + LVDS dual-display function.

Network Function

This board provides two 10/100/1000Mbps Ethernet port to provide users with high-speed and stable network platform selection.

Power Features

AT power, single 5V power supply.

Expansion Bus

Support standard PC104 expansion bus.

IDE Function

One 44Pin IDE hard disk interface and one TYPE I CF card interface; two SATA interface;

I/O Function

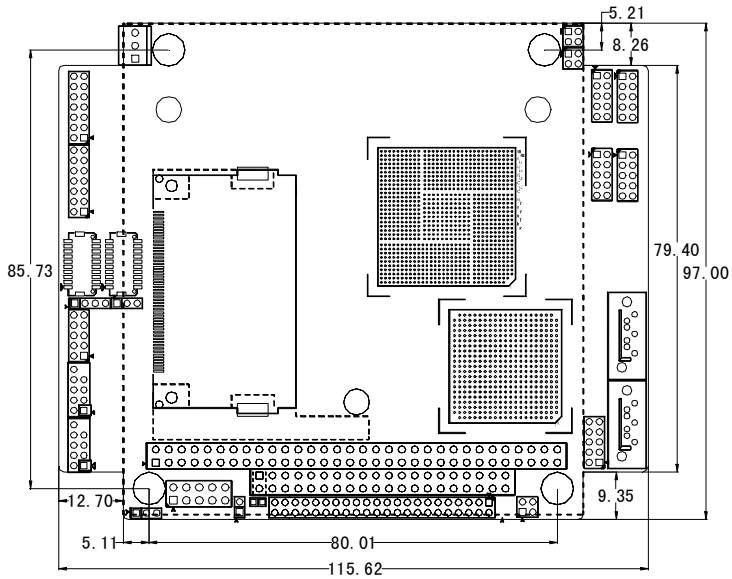
- Two USB2.0 interfaces, they can support four USB devices at the same time.
- 4 serial ports, COM1 and COM2 support RS232 mode while COM3 and COM4 support RS422/RS485 mode;
- One programmable digital I/O interface (4-lane input and 4-lane output).

Watchdog Function

- 255 levels, programmable, time by second;
- Overtime interrupt or system reset.

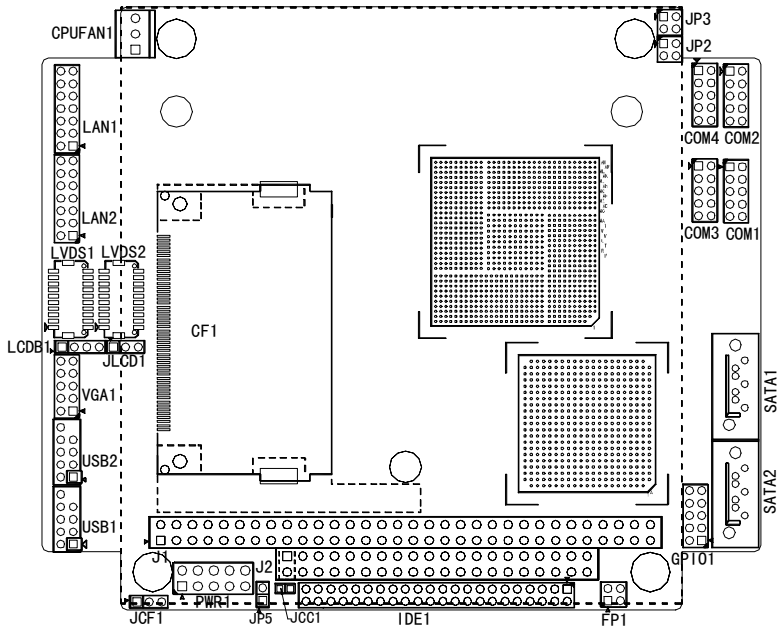
Chapter 2 Installation

Product Dimension Drawing



(Unit: mm)

Locations of Interfaces



Jumper Function Setup

1. JCC1: Clear/Keep CMOS Settings

CMOS is powered by the button battery on board. Clear CMOS will restore original settings (factory default). The steps are listed as follows:

- (1) Turn off the computer and unplug the power cable;
- (2) Instantly short JCC1;
- (3) Turn on the computer;
- (4) Follow the hint on screen to enter BIOS setup when starting the computer, load optimized defaults;
- (5) Save and exit setup mode.



JCC1

Setup	Function
1-2 Open	Normal Operation (Default)
1-2 Short	Clear the content of CMOS, all the BIOS setting resume to factory default value.

2. Serial Ports RS-422/485 Mode Selection

COM3 and COM4 support RS422/485 transmitting mode only, their corresponding jumpers are JP2 and JP3; users can select the mode of COM3 and COM4 by JP2 and JP3.



JP2, JP3

Mode Selection	Pin Setup	
	1-2	3-4
RS-422	OFF	ON
RS-485 (Default)	ON	OFF

Note: ON means Short; OFF means Open.

3. CF Card Selection: Master or Slave

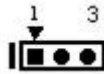


JP5

Setup	Function
1-2 Short	Master
1-2 Open	Slave (Default)

4. LCD Operating Voltage Selection

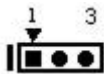
Different LCD screens have different voltages; the board provides two voltage options, 3.3V and 5V. Only when the selected LCD voltage is in accord with the using LCD voltage, the LCD screen could display normally.



JLCD1

Setup	Function
1-2 Short	+3.3V (Default)
2-3 Short	+5V

5. CF Card Voltage Selection



JCF1

Setup	Function
1-2 Short	+3.3V
2-3 Short	+5V (Default)

LCD Backlight Controlling



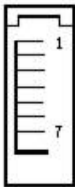
LCDB1

Pin	Signal Name
1	VCC_LCDBKLT
2	LCD_BKLTCTL
3	LCD_BKLTEN
4	GND

Note: VCC_LCDBKLT---backlight power (power voltage is controlled by backlight voltage jumper selection);

LCD_BKLTCTL---backlight controlling; LCD_BKLTEN ----backlight enabling

SATA Interface



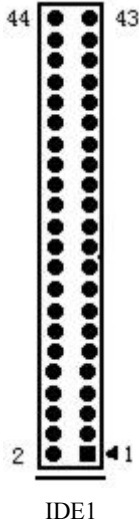
SATA1, SATA2

Pin	Signal Name
1	GND
2	TX+
3	TX-
4	GND
5	RX-
6	RX+
7	GND

IDE Interface

The board provides a set of parallel IDE interface. Pay attention as follows when installing the IDE device:

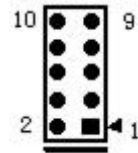
The IDE interface could be connected with only one IDE device. The motherboard provides corresponding jumper to configure it to be used as a master or a slave. When IDE is used as a master, the CF card is a Slave; contrarily, the CF card is a master.



Pin	Signal Name	Pin	Signal Name
1	RESET#	2	GND
3	D7	4	D8
5	D6	6	D9
7	D5	8	D10
9	D4	10	D11
11	D3	12	D12
13	D2	14	D13
15	D1	16	D14
17	D0	18	D15
19	GND	20	Key
21	DREQ	22	GND
23	IOW#	24	GND
25	IOR#	26	GND
27	IORDY	28	GND
29	DACK#	30	GND
31	IRQ	32	NC
33	DA1	34	ATA66_DET
35	DA0	36	DA2
37	CS1#	38	CS3#
39	LED#	40	GND
41	+5V	42	+5V
43	GND	44	GND

USB Interface

This board provides two USB interfaces, which can be connected with four standard USB devices.



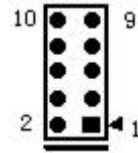
USB1, USB2

Pin	Signal Name	Pin	Signal Name
1	+5V	2	+5V
3	USB1_Data-	4	USB2_Data-
5	USB1_Data+	6	USB2_Data+
7	GND	8	GND
9	NC	10	GND_CHASSIS

Video Interface

1. 10Pin pin-type VGA Interface

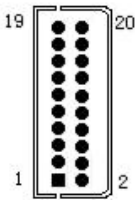
Transfer cable is needed to connect standard VGA device, the pin definitions are listed as follows:



VGA1

Pin	Signal Name	Pin	Signal Name
1	VSYNC	2	HSYNC
3	DDCDATA	4	Red
5	DDCCLK	6	Green
7	+5V	8	Blue
9	GND	10	GND

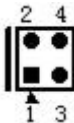
2. Dual-channel (18bit) LVDS Interface



LVDS1, LVDS2

Pin	Signal Name	Pin	Signal Name
1	LVDS_D0+	2	LVDS_D0-
3	GND	4	GND
5	LVDS_D1+	6	LVDS_D1-
7	GND	8	GND
9	LVDS_D2+	10	LVDS_D2-
11	GND	12	GND
13	CLK+	14	CLK-
15	GND	16	GND
17	NC	18	NC
19	VDD	20	VDD

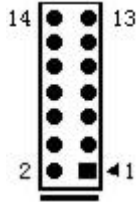
Multi-function Interface



Pin	Signal Name	Pin	Signal
1	SPEAK-	2	+5V
3	RESET	4	GND

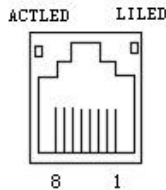
LAN Port

This board provides two 2×7-Pin 10/100/1000Mbps LAN ports, and transfer cable is needed to fix these ports on the chassis, so that they can be connected with the peripheral equipments. The pin definitions are listed as follows:



LAN1, LAN2

Pin	Signal Name	Pin	Signal Name
1	MX0	2	MX0-
3	MX1+	4	MX1-
5	MX2+	6	MX2-
7	MX3+	8	MX3-
9	GND	10	GND
11	LINK_LED+	12	LINK_LED-
13	ACT_LED+	14	ACT_LED-

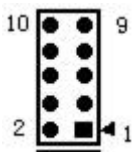


MX0+ (Pin#1)
MX0- (Pin#2)
MX1+ (Pin#3)
MX2+ (Pin#4)
MX2- (Pin#5)
MX1- (Pin#6)
MX3+ (Pin#7)
MX3- (Pin#8)

ACTLED (Single Color: Green)	LAN Activity Indicating Status	LILED (Dual-color: Yellow/Green)	LAN Speed Indicating Status
		Green	1000Mbps
Flash	Data Transmitting	Yellow	100Mbps
Off	No Data to Transmit	Off	10Mbps

Digital I/O Interface

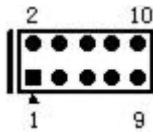
The motherboard provides 4-lane input, 4-lan output GPIO interface.



GPIO1

Pin	Signal Name	Pin	Signal Name
1	INPUT0	2	OUTPUT0
3	INPUT1	4	OUTPUT1
5	INPUT2	6	OUTPUT2
7	INPUT3	8	OUTPUT3
9	GND	10	NC

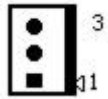
Power Interface



PWR1

Pin	Signal Name	Pin	Signal Name
1	GND	2	+5V
3	NC	4	+12V
5	-5V	6	-12V
7	GND	8	+5V
9	GND	10	+5V

Fan Interface

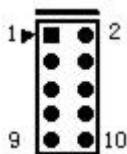


CPUFAN1

Pin	Signal Name
1	GND
2	+5V
3	NC

Serial Port

The motherboard provides four 2 x 5 pin serial ports, all of which are standard pin-type interfaces and need to be fixed onto the chassis via transfer cable to connect with peripheral equipment. COM1 and COM2 support RS-232 mode while COM3 and COM4 support RS-422/RS-485 mode, optional.



COM1~COM4

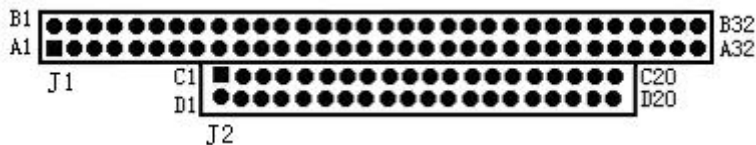
Pin	Signal Name (COM1, COM2)	Signal Name (COM3, COM4)	
	RS-232	RS-422	RS-485
1	DCD#	TXD-	Data-
2	RXD	TXD+	Data+
3	TXD	RXD+	X
4	DTR#	RXD-	X
5	GND	GND	GND
6	DSR#	X	X
7	RTS#	X	X
8	CTS#	X	X
9	RI#	X	X
10	NC	NC	NC

CF Card

Compact Flash card is a rapid storage, which is small in size and easy to use. Its storage capacity varies with different cards, like 128M, 256M, etc. CF card could only be inserted in one direction.

Pin	Signal Name	Pin	Signal Name
1	GND	26	CD1#
2	D3	27	D11
3	D4	28	D12
4	D5	29	D13
5	D6	30	D14
6	D7	31	D15
7	CS0#	32	CS1#
8	GND	33	VS1#
9	ATASEL#	34	IOR#
10	GND	35	IOW#
11	GND	36	WE#
12	GND	37	IRQ
13	VCC	38	VCC
14	GND	39	CSEL#
15	GND	40	VS2#
16	GND	41	RESET#
17	GND	42	IORDY
18	A2	43	DREQ
19	A1	44	DACK#
20	A0	45	DASP#
21	D0	46	ATA66_DET
22	D1	47	D8
23	D2	48	D9
24	WP/IOCS16#	49	D10
25	CD2#	50	GND

PC104 Interface



Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	IOCHCK#	B1	GND	C1	GND	D1	GND
A2	SD7	B2	RESET	C2	SBHE#	D2	MEMCS16#
A3	SD6	B3	+5V	C3	LA23	D3	IOCS16#
A4	SD5	B4	IRQ9	C4	LA22	D4	IRQ10
A5	SD4	B5	-5V	C5	LA21	D5	IRQ11
A6	SD3	B6	DRQ2	C6	LA20	D6	IRQ12
A7	SD2	B7	-12V	C7	LA19	D7	IRQ15
A8	SD1	B8	SRDY#	C8	LA18	D8	IRQ14
A9	SD0	B9	+12V	C9	LA17	D9	DACK0#
A10	IOCHRDY	B10	KEY	C10	MEMR#	D10	DRQ0
A11	AEN	B11	SMEMW#	C11	MEMW#	D11	DACK5#
A12	SA19	B12	SMEMR#	C12	SD8	D12	DRQ5
A13	SA18	B13	IOW#	C13	SD9	D13	DACK6#
A14	SA17	B14	IOR#	C14	SD10	D14	DRQ6
A15	SA16	B15	DACK3#	C15	SD11	D15	DACK7#
A16	SA15	B16	DRQ3	C16	SD12	D16	DRQ7
A17	SA14	B17	DACK1#	C17	SD13	D17	+5V
A18	SA13	B18	DRQ1	C18	SD14	D18	MASTER#
A19	SA12	B19	REFRESH#	C19	SD15	D19	GND
A20	SA11	B20	BCLK	C20	KEY	D20	GND
A21	SA10	B21	IRQ7				
A22	SA9	B22	IRQ6				
A23	SA8	B23	IRQ5				
A24	SA7	B24	IRQ4				
A25	SA6	B25	IRQ3				
A26	SA5	B26	DACK2#				
A27	SA4	B27	TC				
A28	SA3	B28	BALE				
A29	SA2	B29	+5V				
A30	SA1	B30	OSC				
A31	SA0	B31	GND				
A32	GND	B32	GND				

Chapter 3 BIOS Setup

Regarding the BIOS features setup of 104-1812CLD2N, please refer to the *AMI BIOS Setup Guide* edited by the manufacturer

Description for Display Driver

Installation of the display driver, operate Setup.exe under IEGD_9_0_2_Windows\Utilities file to install or uninstall the driver.

Users can configure the display driver (single-display, dual-display) via operating IEGDGUI.exe under IEGD_9_0_2_Windows\Utilities file or carry out configuration via the advanced options in display property.

Appendix

Watchdog Programming Guide

104-1812CLD2N provides a programmable watchdog timer (WDT) up to 255 levels and time by minute or second. Watchdog timer overtime event can be programmed to reset system or generate shielding interrupts.

The following describes WDT program in C language. Note: before operating WDT, users shall firstly enter WDT programming mode; after finish configuring WDT, exit WDT.

The steps to program WDT are as follows:

- enter WDT programming mode
- setup WDT operating mode/enable WDT/disable WDT
- exit WDT programming mode

The following files shall be included:

```
#include <stdio.h>
#include <dos.h>
#include <bios.h>
#include <stdlib.h>
#include <string.h>
```

(1) Enter WDT programming mode

```
outportb(0x2e,0x67); //Enter WDT programming mode, write 67 on INDEX PORT
                        for twice

outportb(0x2e,0x67); //INDEX PORT [4e /2e], DATA PORT[4F/2F]
outportb(0x2e,0x07); //reg0X07, used to select logic device
outportb(0x2f,0x08); //select logic device8,
```

```
outportb(0x2e,0x30); //reg0x30, device enables register, 0=disable, 1=enable
```

```
outportb(0x2f,0x01); //enable watchdog timer
```

(2) Setup WDT operating mode, reset mode or interrupt mode:

```
outportb(0x2e, 0x70);
```

```
char oldval = inportb(0x2f);
```

a. Configure WDT to reset mode only

```
oldval &= 0xef;          /*reg0x70.bit[4] set this bit to 0 only in reset mode
```

```
0=WDTO
```

```
*/
```

```
outportb(0x70, oldval);
```

b. Configure WDT to interrupt and reset mode

```
oldval |= 0x10;
```

```
oldval |= IRQ_RESOURCE;          /*reg0x70.bit[4] set this bit to 1 in reset and
```

```
interrupt mode
```

```
1=WDTO and IRQ
```

```
bit[3:0]WDT interrupt Mapping
```

```
available interrupts: 03h~05h,09h~0bh, other interrupts
```

```
is not available
```

```
03h = IRQ3
```

```
04h = IRQ4
```

```
.....
```

```
*/
```

```
outportb(0x70, oldval);
```

(3)WDT timer selection: minute or second

a. Select to time by minute with the following words:

; suppose it is under WDT programming mode

```
outportb(0x2e,0xf0); //select to time by minute, register 0xf0.bit[2:1]=10。
```

```
outportb(0x2f,0x04);
```

b. Select to time by second with the following words:

; suppose it is under WDT programming mode

```
outportb(0x2e,0xf0); //select to time by second, register 0xf0.bit[2:1]=01
```

```
outportb(0x2f,0x02);
```

(4) Enable/Disable WDT

; suppose it is under WDT programming mode

```
outportb(0x2e,0xf1);
```

```
outportb(0x2f,TIME-OUT-VALUE);
```

```
outportb(0x2e,0xf1);
```

```
outportb(0x2f,TIME-OUT-VALUE); //write-in the preset time TIME-OUT-VALUE  
for twice
```

Note: the range of TIME-OUT-VALUE is from 1 to 255, the unit is “second” or “minute”.

WDT will be enabled after writing TIME-OUT-VALUE to register for twice, or,
WDT will be disabled.

If TIME-OUT-VALUE is zero, WDT is disabled.

(5) Exit WDT Programming Mode

```
outportb (0x2e,0xaa) ;
```

GPIO Programming Guide

This motherboard educes 8 pins by chipset PCA 9534. On hardware, the default setup of these 8 pins are all input, users can set it to input or output by software program.

Necessary constant parameter and the description for the using register

PCI space: Bus: 0, Dev: 31, fun: 3; Reg: 20~23---used to read SMBUS I/O space basic address BAR

PCA9534 address slave_adr=0x20;	Reg: 40 Bit [2] I2C_EN bit the high 7 bits of the 8 bit address, bit[7:1], is hardware setup address 0x20, the last bit is used to setup read and write function, bit[0]=0, write; bit[0]=1, read;
0x40	address and write command, used to modify the value of GPIO controlling register
0x41	address and read command, used to read the value of GPIO controlling register

Four GPIO controlling registers

0x00-input port (Read), the corresponding pin is high level when the value of bit7~bit0 is 1; and it is low level when the value is 0.

0x01-output port (Read/Write), the corresponding pin is high level when the value of bit7~bit0 is 1; and it is low level when the value is 0.

0x02-Polarity Inversion (Read/Write), the default value is 0x00, when the value of bit7~bit0is 1, polarity inversion.

0x03-Configuration(Read/Write), the default value is 0xff, enable/disable output/input function, when the value of bit7~bit0 is 1, the output function of corresponding pin is disabled, and input function is enabled; when the value of bit7~bit0 is 0, the output function of corresponding pin is enabled, and input function is disabled.

Five SMBUS register:

BAR+Offset 0x00: HST_STS status register

BAR+Offset 0x02: HST_CNT controlling register

BAR+Offset 0x03: HST_CMD command register, Bit [7:0] is used to select GPIO controlling register

BAR+Offset 0x04: XMIL_SLAVE address register, Bit[7: 0] is used to write-in Slave Address and read-write bit

BAR+Offset 0x05: DATA0: data register, it is used to store the received and sent data.

Program Controlling Process

1. Read the basic address, enter PCI configure space, read Smbus address BAR, and set 0 to I2C_EN bit;
2. write GPIO controlling register: enter Smbus I/O space, write 0xbf to HST_STS, clear the status bit, set 010 to bit [4:2] of HST_CNT register, write 0x40 (write command) to XMIL_SLAVE register, write GPIO controlling register 0x03 to HST_CMD, write 0x0f to DATA0, modify the value of GPIO controlling register 0x03 to 0x0f, and set GP1, 3, 5, 7 to output, set GP2, 4, 6, 8 to input;
3. Begin: set 1 to HST_CNT bit[6]START, begin to transmit address, command and data, circularly read HST_STS status register, when bit[2]DEV_ERR is set to 1, it means transmitting error; when bit[1]INTR is set to 1, it means transmitting completion, and the next step can be carried out;
4. Imitate step 2, users can modify other GPIO controlling register;
5. Read GPIO controlling register: enter Smbus I/O space, write 0xbf to HST_STS, clear status bit, set 010 to bit[4:2] of HST_CNT register, write 0x41 (read command) to XMIL_SLAVE register, write GPIO controlling register 0x00 to HST_CMD;
6. Begin: set 1 to HST_CNT bit[6]START, begin to transmit address, command and data, circularly read HST_STS status register, when bit[2]DEV_ERR is set to 1, it means transmitting error, when bit[1]INTR is set to 1, it means transmitting completion, then the input register, namely, the level of input pin is stored in DATA0 register, read DATA0 register to get the level of input pin.

Users can setup the input/output pin and high/low level according to the program process above.

I/O Address Map

There is 64K for the system I/O address space. Each external device will occupy portion of the space. The table below shows parts of the distribution of the I/O address. As the address of PCI device (e.g. PCI network card) is configured by software, it is not listed in this table.

Address	Device Description
000h - 00Fh	DMA Controller#1
020h - 021h	Programmable Interrupt Controller#1
040h - 043h	System Timer
060h - 064h	Standard 101/102 Keyboard Controller
070h - 071h	Real-Time Clock NMI
081h - 08Fh	DMA Page Register
0A0h - 0A1h	Programmable Interrupt Controller#2
0C0h - 0DEh	DMA Controller#2
0F0h - 0FFh	Numeric Data Processor
170h - 177h	Slave IDE
1F0h - 1F7h	Master IDE
200h - 207h	Serial Port #3(COM3)
208h-20Fh	Serial Port #4(COM4)
2F8h - 2FFh	Serial Port #2(COM2)
376h	Slave IDE(dual FIFO)
378h - 37Fh	Parallel Port#1 (LPT1)

IRQ Assignment Table

The system has 12 interrupt sources; some are occupied by system devices. Only the ones which are not occupied can be assigned to other devices. The ISA devices claim to engross the interrupt; only the plug and play ISA devices can be assigned by the BIOS or the OS. Multiple PCI devices can share the same interrupt, and are assigned by BIOS or OS. The following table shows the interrupt assignment for parts of the devices of this CPU card, but the interrupt sources occupied by PCI device are not listed.

Level	Function
IRQ0	System Timer
IRQ1	Standard 101/102 key or Microsoft PS/2 keyboard
IRQ2	Programmable Interrupt Controller
IRQ3	Serial Port #3 and #4
IRQ4	Serial Port #1 and #2
IRQ5	Reserved
IRQ6	Reserved
IRQ7	Reserved
IRQ8	System CMOS/Real-time Clock
IRQ9	SCI IRQ used by ACPI bus
IRQ10	Reserved
IRQ11	Reserved
IRQ12	PS/2 Mouse
IRQ13	Numeric data processor
IRQ14	Master IDE
IRQ15	Slave IDE