

User Manual



PCI-7031

Intel[®] Atom[™] Dual-Core D510/ Fanless N450 CPU, PCI Half-size SBC with on-board DDR2 / VGA / LVDS / Dual-GbE / SATA / COM

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Certifications

CE

FCC Class A

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A Message to the Customer

Technical support

We want you to get the maximum performance from your products. So if you run into technical difficulties, we are here to help. For the most frequently asked questions, you can easily find answers in your product documentation. These answers are normally a lot more detailed than the ones we can give over the phone.

So please consult this manual first. If you still cannot find the answer, gather all the information or questions that apply to your problem, and with the product close at hand, call your dealer. Our dealers are well trained and ready to give you the support you need to get the most from your products. In fact, most problems reported are minor and are able to be easily solved over the phone.

In addition, free technical support is available from [* | engineers every business day. We are always ready to give advice on application requirements or specific information on the installation and operation of any of our products.

Product Warranty (2 years)

V@Á æj æšc '^ warrants to you, the original purchaser, that each of its products 引為free from defects in materials and workmanship for two years from the date [本 h chase.

If you think you have a defective product, follow these steps:

- Collect all the information about the problem encountered. (For example, CPU speed, other hardware and software used, etc.) Note anything abnormal and list any onscreen messages you get when the problem occurs.
- 2. Call your dealer and describe the problem. Please have your manual, product, and any helpful information readily available.
- 3. If your product is diagnosed as defective, obtain an RMA (return merchandise authorization) number from your dealer. This allows us to process your return more quickly.
- 4. Carefully pack the defective product, a fully-completed Repair and Replacement Order Card and a photocopy proof of purchase date (such as your sales receipt) in a shippable container. A product returned without proof of the purchase date is not eligible for warranty service.
- 5. Write the RMA number visibly on the outside of the package and ship it prepaid to your dealer.

Before you begin installing your single board computer, please make sure that the following materials have been shipped:

If any of these items are missing or damaged, contact your distributor or sales representative immediately.

We have carefully inspected the PCI-7031 mechanically and electrically before shipment. It should be free of marks and scratches and in perfect working order upon receipt.

As you unpack the PCI-7031, check it for signs of shipping damage. (For example, damaged box, scratches, dents, etc.) If it is damaged or it fails to meet the specifications, notify our service department or your local sales representative immediately. Also notify the carrier. Retain the shipping carton and packing material for inspection by the carrier. After inspection, we will make arrangements to repair or replace the unit.

Initial Inspection

Before you begin installing your single board computer, please make sure that the following materials have been shipped:

1 PCI-7031D(N)-S6A1E single board computer	
1 CPU Cooler for Atom D510 CPU (Only Available for D SKU)	P/N: 1960046526N001
1 PCI-7031 Startup Manual	
1 CD with driver utility and manual (in PDF format)	
1 FDD cable	P/N: 1700340640
1 Ultra ATA 66/100 HDD cables	P/N: 1701400452
2 Serial ATA HDD data cable	P/N: 1700003194
2 Serial ATA HDD power cable	P/N: 1703150102
1 Printer (parallel) port cable kit	P/N: 1701260301
1 Dual COM ports cable kit	P/N: 1700008762
1 ATX Feature Cable	P/N: 1700002343
1 4-Port USB cable kit	P/N: 1700008887
1 Y cable for PS/2 keyboard and PS/2 mouse	P/N: 1700060202
1 AT/ATX PSU 20-Pin to 12-Pin Cable Kit	P/N: 1700000265
1 Jumper Pack	P/N: 9689000068
1 Warranty card	

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Note!



Using PCI-7031D's proprietary CPU cooler included in its package is a must. Other brands of CPU coolers are NOT compatible with PCI-7031. PCI-7031N is of fanless CPU type and does not need installing a CPU cooler by user.

Verified Memory List

Brand	Size	Speed	Туре	ECC	Vendor PN		Memory
	256 MB	DDR2 667	SODIMM DDR2	N	TS32MSQ64V6M	Ж	Hynix HY5PS121621B FP-Y5 (32x16)
Tran- scend	512 MB	DDR2 667	SODIMM DDR2	N	TS6QSJ23002-6S/ TS64MSQ64V6J	Á Á Á	SAMSUNG K4T51083QC ZCE6 (64x8)
	512 MB	DDR2 667	SODIMM DDR2	N	Hynix HY5PS121621B FP-Y5	Á	Hynix HY5PS121621B FP-Y5 (32x16)
	1 GB	DDR2 667	SODIMM DDR2	N	TS128MSQ64V6J	ÁÁ	SAMSUNG K4T51083QC ZCE6 (64x8)
	2 GB	DDR2 667	SODIMM DDR2	N	TS5QSU27300-6M	ÁÁ ÁÁ	Micron D9HNL (128x8)
Anger	512 MB	DDR2 667	SODIMM DDR2	N	78.92G63.422	ÁÁ	ELPIDA E5108AG-6E-E (64x8)
Apacer	1 GB	DDR2 667	SODIMM DDR2	N	78.02G63.423	ÁÁ Á	ELPIDA E5108AGBG-6E-E (64x8)
	256 MB	DDR2 667	SODIMM DDR2	N	NA	Á	ELPIDA E5116AF-6E-E (32x16)
	512 MB	DDR2 667	SODIMM DDR2	N	NA		ELPIDA E5108AGBG-6E-E (64x8)
	1 GB	DDR2 667	SODIMM DDR2	N	NA		ELPIDA E5108AGBG-6E-E (64x8)
DCI	2 GB	DDR2 667	SODIMM DDR2	N	NA		ELPIDA E1108ACSE-6E-E (128x8)
DSL	1 GB	DDR2 800	SODIMM DDR2	N	TS64MSQ64V6M	Á	Hynix HY5PS121621B FP-Y5 (32x16)
	2 GB	DDR2 800	SODIMM DDR2	N	TS256MSQ64V8U	Á	Micron D9HNP (128x8)
	1 GB	DDR2 800	SODIMM DDR2	N	NA		ELPIDA TWN E5108AHSE-8E- E (64x8)
	2 GB	DDR2 800	SODIMM DDR2	N	NA		ELPIDA JPN E1108ACSE-8E-E (128x8)

Certification and Safety Instructions

This device complies with the requirements in part 15 of the FCC rules: Operation is subject to the following two conditions:

- 1. This device may not cause harmful interference, and
- 2. This device must accept any interference received, including interference that may cause undesired operation

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this device in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his/her own expense. The user is advised that any equipment changes or modifications not expressly approved by the party responsible for compliance would void the compliance to FCC regulations and therefore, the user's authority to operate the equipment.



Caution! There is a danger of a new battery exploding if it is incorrectly installed. Do not attempt to recharge, force open, or heat the battery. Replace the battery only with the same or equivalent type recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions.

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Chapter

Hardware Configuration

1.1 Introduction

PCI-7031 is an Atom dual-core D510 / fanless N450 CPU based PCI-interface half-size PICMG single board computer. With high performance Atom D510 dual-core computing power, it is ideal for intense data or graphic processing applications; with fanless Atom N450 CPU and on-board memory feature, it has ultra high reliability to resist heat, dust, vibration and shock in any application environment.

PCI-7031 is designed with an Intel® Atom™ D510/N450 CPU and ICH8M I/O control hub. The Atom D510 dual core CPU brings new generation computing capability into the half-size SBC application field. Compact size, low power consumption (Total power consumption ≤17.796 W) and dual-core parallel computing power and maximum 2 GB of DDR2 667 MHz memory capacity makes the PCI-7031D a powerful small form-factor computer platform for modern industrial applications that require high computing power. The fanless Atom N450 CPU (Total power consumption ≤ 15.264 W) and on-board memory design eliminate moving fan parts and memory socket connections; this makes PCI-7031N ultra reliable to conduct its mission under various kinds of high-temperature, vibrating, shocking and dusty harsh environments.

PCI-7031 has an integrated graphic core of Intel Embedded Gen3.5+ graphic technology with 224 MB shared memory. This feature makes PCI-7031 is capable of handling complex and intense 2D/3D graphic processing without an add-on graphic card; its VGA and LVDS dual video outputs also makes it suitable for applications requiring dual display or digital panel display capabilities.

PCI-7031 is rich in I/O interfaces: it has three SATA ports (300 MB/sec) for mainstream SSD (solid state disk), HDD, and ODD connections, one legacy IDE port for the ODD connection. It also has a CF socket to support an economical, easy-tomaintain SSD device. Additionally, the dual Gigabit Ethernet LANs with teaming functions offer strong networking capability; the two serial ports (COM ports) can be used as reliable legacy device control interfaces.

1.2 Features

- Complies with PICMG[®] 1.0
- Ultra low power (Total Power Consumption ≤15.264 W), fanless N450 CPU and 1 GB on-board DDR2 667 memory (Only for N SKU)
- Dual-core high performance D510 CPU and maximum 2 GB DDR2 667 memory (Only for D SKU)
- Intel® Embedded Gen3.5+ graphics core with 224 MB of shared memory with VGA/LVDS dual video outputs (supporting mirror (clone) and extension modes)
- Supports Dual-Gigabit Ethernet LANs with teaming capability
- Supports Embedded Software SUSI APIs and Utilities. (SUSI APIs: watchdog, hardware monitor, brightness control, programmable GPIO, backlight On/Off; Utilities: BIOS flash, eSOS, system monitoring, Flash Lock, software protection)

1.3 Specifications

1.3.1 **System**

- CPU: Soldered-down (BGA type) Intel Atom 1.66GHz D510 dual-core CPU or 1.66GHz N450 fanless CPU
- L2 Cache: CPU built-in 512 KB / 1 MB L2 cache
- BIOS: AMI Flash BIOS
- System Chipset: Intel[®] ICH8M
- SATA/EIDE hard disk drive interface: Supports up to 3 independent Serial ATA hard drives (up to 300 MB/s) as well as one IDE port (maximum 2 devices)
- Floppy disk drive interface: Supports up to two floppy disk drives, 5¹/₄ (360 KB and 1.2 MB) and/or 3¹/₂ (720 KB, 1.44 MB). BIOS enabled/disabled.

1.3.2 Memory

- RAM:
 - N SKU: 1GB on-board DDR2 667 MHz memory
 - D SKU: Maximum 2 GB DDR2 667 MHz memory in SO-DIMM socket

Note!



PCI-7031 is ONLY compatible with DDR2 memory modules that are assembled with x16 (16-bit) memory chips and NOT compatible with those that are assembled with x8 (8-bit) memory chips. Using wrong memory modules may cause unexpected system instability.

1.3.3 Input/Output

- Bus interface: PICMG[®] 1.0 compliant bus interface
- PCI Bus: Four 32bit / 33 MHz PCI masters to backplane
- Enhanced parallel port: Configurable to LPT1, LPT2, LPT3, or disabled. Standard DB-25 female connector provided. Supports EPP/SPP/ECP
- Serial ports: Two RS-232 ports
- **Keyboard and PS/2 mouse connector:** One 6-pin mini-DIN connector is located on the mounting bracket for easy connection to a keyboard or PS/2 mouse. An on board keyboard pin header connector is also available
- **High Definition Audio:** PCI-7031 can provide audio function with the optional audio extension module PCA-AUDIO-HDA1E
- **USB ports**: PCI-7031 supports up to 7 USB 2.0 ports with transmission rates up to 480 Mbps

1.3.4 Graphic interface

- Controller: Integrated graphic core of Embedded Gen3.5+ technology
- VRAM: 224 MB shared system memory
- Output Interfaces:
 - VGA: Supports up to SXGA 1400 x 1050 @ 60Hz for Atom N450, up to 2048 x 1536 @ 60 Hz for Atom D510
 - LVDS: Supports 18-bit single channel and up to WXGA 1366 x 768 or 1280 x 800 for both Atom D510 and N450 CPUs
 - Dual Display: CRT + LVDS, supports extended mode and clone mode

1.3.5 Ethernet LAN

- Supports dual10/100/1000 Mbps Ethernet networking
- Controller: LAN 1: Intel[®] 82567V; LAN 2: Intel[®] 82583V

1.3.6 Industrial features

- Watchdog timer: Can generate a system reset. The watchdog timer is programmable, with each unit equal to one second or one minute (255 levels). You can find programming details in Appendix A
- Fanless N450 CPU and on-board 1GB DDR2 memory for N SKU for ultra high reliability and long MTBF

1.3.7 Mechanical and environmental specifications

- Operating temperature: 0 ~ 60° C (32 ~ 140° F, depending on CPU)
- **Storage temperature:** -20 ~ 70° C (-4 ~ 158° F)
- Humidity: 20 ~ 95% non-condensing
- Demanded Power supply voltage: +12 V, +5 V, +5 VSB
- Power consumption:
 - D SKU:

CPU: Dual-core Atom D510 CPU 1.66 GHz

Memory: 1 Piece of 2 GB DDR2 667 MHz SO-DIMM **Storage:** One IDE HDD and one SATA CD ROM

Test program: BurnIn Test 6.0

+12 V: 0.228 A +5 V: 2.952 A +3.3 V: 0 A +5 VSB: 0.06 A -12 V: 0 A -5 V: 0 A

Total Power Consumption: 17.796 W

- N SKU:

CPU: Single Core Atom N450 CPU 1.66 GHz **Memory:** On-board 1GB DDR2 667 Memory **Storage:** One IDE HDD and one SATA CD ROM

Test Program: BurnIn Test 6.0

+12 V: 0.192 A +5 V: 2.532 A +3.3 V: 0 A +5 VSB: 0.060 A -12 V: 0 A

Total Power Consumption: 15.264 W

■ **Board size:** 185 mm (L) x 122 mm (W) (7.3" x 4.8")

■ **Board weight:** 0.5 kg (1.2 lb)

1.4 Jumpers and Connectors

Connectors on the PCI-7031 single board computer link it to external devices such as hard disk drives and a keyboard. In addition, the board has a number of jumpers used to configure your system for your application.

Below, Tables 1.1 and 1.2 list the jumper and connector functions. Later sections in this chapter give instructions on setting jumpers. Chapter 2 gives instructions for connecting external devices to your single board computer.

Table 1.1: Jumper descriptions			
Label	Function		
CMOS1	CMOS Clear		
JWDT1	Watchdog timer output option		

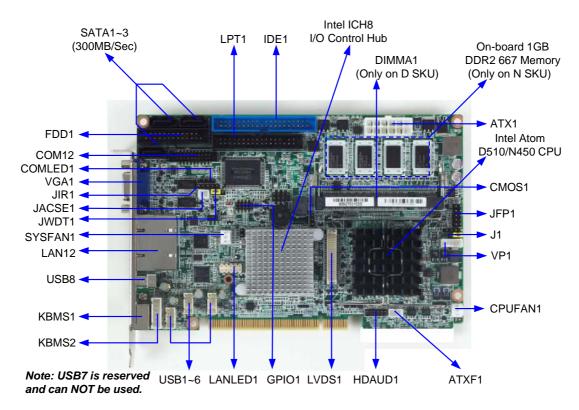
Table 1.2: Connect	or descriptions
Label	Function
IDE1	Primary IDE connector
FDD1	Floppy drive connector
LPT1	Parallel port
VGA1	VGA connector
LVDS1	LVDS Pin-header
COM12	Serial port 1~2 (2.00 pitch box header)
KBMS1	PS/2 keyboard and mouse connector
KBMS2	External keyboard/mouse pin header
JIR1	Infrared port pin header
CPUFAN1	3-pin Atom D510 CPU fan connector

Table 1.2: Connect	tor descriptions
SYSFAN1	3-pin System fan connector
JFP1	Power and Reset Button connector
LAN12	Dual Giga LAN RJ45 connector with Transformer
HDAUD1	High Definition Audio interface connector
SATA1	Serial ATA1
SATA2	Serial ATA2
SATA3	Serial ATA3
USB 12	USB port 1 and port 2 pin-header
USB 34	USB port 3 and port 4 pin-header
USB 56	USB port 5 and port 6 pin-header
USB8	The 7th USB port on rear bracket
LANLED1	LAN1 and LAN2 LED connector
GPIO1	GPIO header

Note! USB7 is reserved and can not be used.



1.5 Board Layout: Jumper and Connector Locations



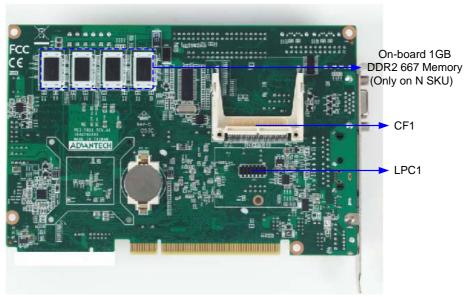


Figure 1.1 Board Layout

1.6 PCI-7031 Block Diagram

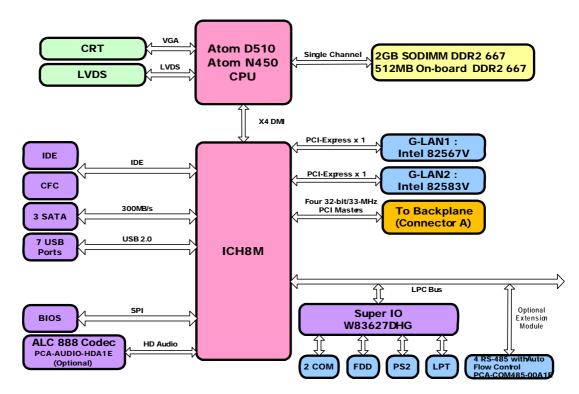


Figure 1.2 Block Diagram

Safety Precautions 1.7



Warning! Always completely disconnect the power cord from your chassis whenever you work with the hardware. Do not make connections while the power is on. Sensitive electronic components can be damaged by sudden power surges. Only experienced electronics personnel should open the PC chassis.



Caution! Always ground yourself to remove any static charge before touching the single board computer. Modern electronic devices are very sensitive to electrostatic discharges. As a safety precaution, use a grounding wrist strap at all times. Place all electronic components on a static-dissipative surface or in a static-shielded bag when they are not in the chassis.



Caution! The computer is provided with a battery-powered real-time clock circuit. There is a danger of explosion if battery is incorrectly replaced. Replace only with same or equivalent type recommended by the manufacturer. Discard used batteries according to manufacturer's instructions.

Note!

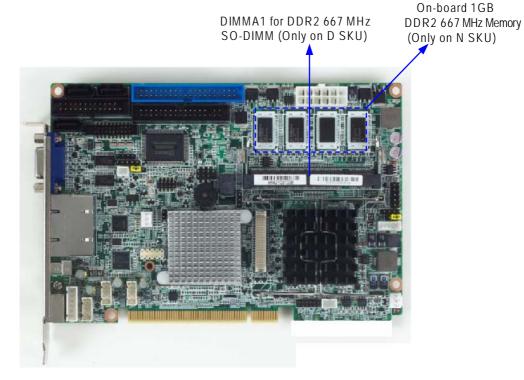


Before installing your PCI-7031 into a chassis, make sure that no components on either side of the CPU card can touch any metal parts, especially the chassis wall and add-on card in the adjacent slot.

The PCI-7031D has one SO-DIMM socket (while PCI-7031N does NOT). PCI-7031 is ONLY compatible with DDR2 memory modules that are assembled with x16 (16-bit) memory chips and NOT compatible with those that are assembled with x8 (8-bit) memory chips. Using wrong memory modules may cause system instability and unexpected behavior.

1.9 Memory Installation Procedures

- 1. See picture below to locate DIMMA1 200-pin SODIMM socket.
- 2. A memory module and expansion socket are keyed. The plastic bridge in the socket must align with the notch in the module. The keyed bridge and notch make sure a SODIMM cannot be installed going the wrong direction.
- Insert the SODIMM module into the socket at a 30-45 degree angle. Make sure
 the notch and the module are properly aligned.
 Slowly push down the SODIMM toward the CPU card PCB until the clips at each
 end of the expansion socket click into place.



9

1.10 Processor Installation

PCI-7031 series are equipped with soldered-down (BGA type) CPUs. no need for a user to install a CPU.

1.11 CPU Cooler Installation

Only PCI-7031D needs to have a CPU cooler installed by user (P/N: 1960046526N001), PCI-7031N does NOT require this; it already has a fanless heatsink assembled on the CPU card.

PCI-7031D users please follow the instructions below to install the CPU cooler which is included in the package.

First locate the Atom D510 CPU then put the metal plate included in CPU cooler package onto the solder side of the PCB with its four legs inserted into these four mounting holes around the CPU, then attach the CPU cooler onto the CPU card by fastening the four screws, one into each leg of the metal plate. Fasten the first screw loosely, then loosely engage the second screw diagonally across from the first one, then half fasten the third, and fourth screws. Finally snug all four screws completely, following the same order.



Warning! Without a fan or heat sink, the CPU will overheat and cause damage to both itself and the single board computer. If you are a D SKU user, please install the CPU cooler (P/N: 1960046526N001) before booting up the system and do NOT remove any on-board passive heat sinks; if you are an N SKU user, please do NOT remove any on-board passive heat sinks.

> Improper CPU cooler installation may cause serious CPU die damage; please follow the instructions above to install your CPU cooler.

Chapter

Connecting
Peripherals & Jumper
Settings

2.1 Introduction

You can access most of the connectors from the top of the board while it is installed in the chassis. If you have a number of cards installed or have a packed chassis, you may need to partially remove the card to make all the connections.

You can configure your single board computer to match the needs of your application by setting the jumpers. A jumper is a metal bridge that closes an electrical circuit. It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To "close" (or turn ON) a jumper, you connect the pins with the clip. To "open" (or turn OFF) a jumper, you remove the clip.

Sometimes a jumper consists of a set of three pins, labeled 1, 2, and 3. In this case, you connect either pins 1 and 2, or 2 and 3. A pair of needle-nose pliers may be useful when setting jumpers.

2.2 IDE Connector (IDE1)

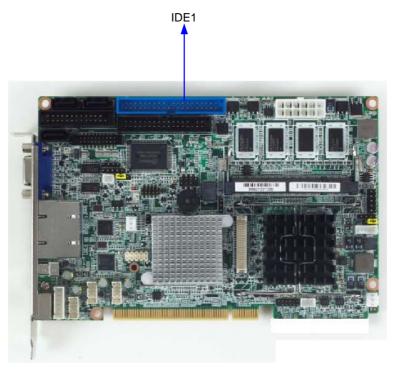


Figure 2.1 PCI-7031 IDE1 location

You can attach up to two IDE (Integrated Drive Electronics) drives to the PCI-7031's built-in controller. The primary connector can accommodate two drives.

Wire number 1 on the cable is red or blue and the other wires are gray. Connect one end to connector IDE1 on the single board computer. Make sure that the red/blue wire corresponds to pin 1 on the connector (in the upper right hand corner). See Chapter 1 for help finding the connector.

Unlike floppy drives, IDE hard drives can connect in either position on the cable. If you install two drives to a single connector, you will need to set one as the master and the other as the slave. You do this by setting the jumpers on the drives. If you use just one drive per connector, you should set each drive as the master. See the documentation that came with your drive for more information.

Connect the first hard drive to the other end of the cable. Wire 1 on the cable should also connect to pin 1 on the hard drive connector, which is labeled on the drive circuit board. Check the documentation that came with the drive for more information.

2.3 Floppy Drive Connector (FDD1)

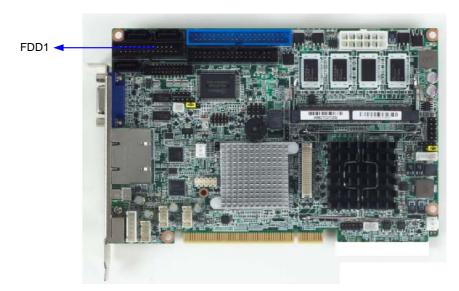


Figure 2.2 PCI-7031 FDD1 location

You can attach up to two floppy disk drives to the PCI-7031's on board controller. You can use 3.5" (720 KB, or 1.44 MB) drives.

The single board computer comes with a 34-pin daisy-chain drive connector cable. On one end of the cable is a 34-pin flat-cable connector. On the other end are two sets of 34-pin flat-cable connector (usually used for 3.5" drives). The set on the end (after the twist in the cable) connects to the A: floppy drive. The set in the middle connects to the B: floppy drive.

2.4 Parallel Port (LPT1)

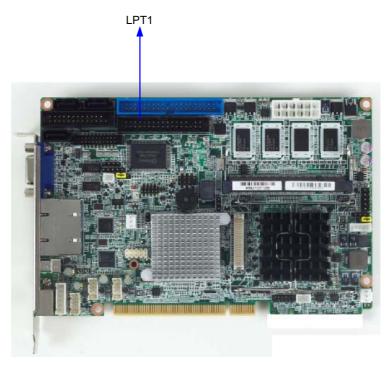


Figure 2.3 PCI-7031 LPT1 location

The PCI-7031 includes an onboard parallel port, accessed through a 26-pin flat-cable connector, LPT1. The card comes with an adapter cable which lets you use a traditional DB-25 connector. The cable has a 26-pin connector on one end and a DB-25 connector on the other, mounted on a retaining bracket. The bracket installs at the end of an empty slot in your chassis, giving you access to the connector.

The parallel port is designated as LPT1, and can be disabled or changed to LPT2 or LPT3 in the system BIOS setup.

To install the bracket, find an empty slot in your chassis. Unscrew the plate that covers the end of the slot. Screw in the bracket in place of the plate. Next, attach the flat-cable connector to LPT1 on the CPU card. Wire 1 of the cable is red or blue, and the other wires are gray. Make sure that wire 1 corresponds to pin 1 of LPT1. Pin 1 is on the upper right side of LPT1.

2.5 VGA Connector (VGA1)



Figure 2.4 VGA Connector (VGA1)

The PCI-7031 includes a VGA interface that can drive conventional CRT displays. VGA1 is a standard 15-pin D-SUB connector commonly used for VGA. Pin assignments for CRT connector VGA1 are detailed in Appendix B.

2.6 Serial Ports (COM12)

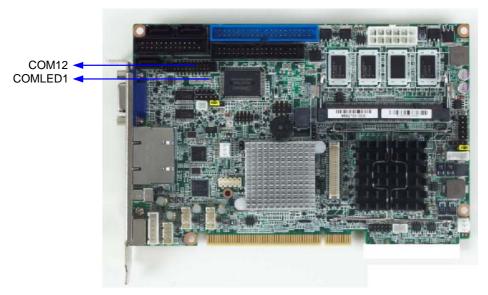


Figure 2.5 Serial Ports (COM12)

The PCI-7031 offers two serial ports: COM1 and COM2. These ports can connect to serial devices, such as a mouse or to a communications network.

You may connect the dual COM ports cable kit 1700008762 to COM12 box-header to have these 2 DB9 RS232 ports on the rear bracket.

The IRQ and address ranges for all ports are fixed. However, if you want to disable the port or change these parameters later, you can do this in the system BIOS setup.

Different devices implement the RS-232 standard in different ways. If you are having problems with a serial device, be sure to check the pin assignments for the connector.

2.7 PS/2 Keyboard/Mouse Connector (KBMS1)

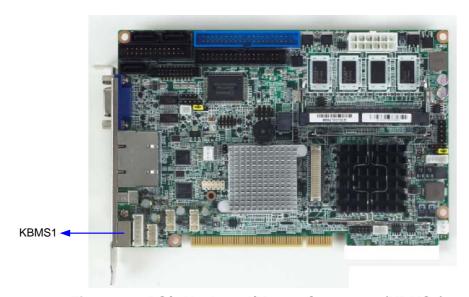


Figure 2.6 PS/2 Keyboard/Mouse Connector (KBMS1)

One 6-pin mini-DIN connector (KBMS1) on the card mounting bracket provides connection to a PS/2 keyboard or a PS/2 mouse, respectively. KBMS1 can also be connected to an adapter cable (P/N: 1700060202) for connecting to both a PS/2 keyboard and a PS/2 mouse.

2.8 External Keyboard Pin Header (KBMS2)

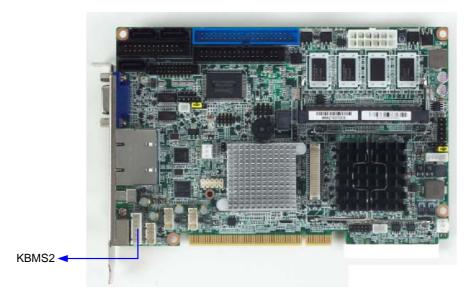


Figure 2.7 External Keyboard Connector (KBMS2)

In addition to the PS/2 mouse/keyboard connector on the PCI-7031's rear plate, there is also an extra onboard external keyboard pin header. This gives system integrators greater design flexibility.

2.9 CPU Fan Connectors (CPUFAN1)



Figure 2.8 CPU Fan Connectors (CPUFAN1)

This connector supplies power and fan speed signal to PCI-7031D's proprietary CPU cooler for Atom D510 CPU.

2.10 Front Panel Connectors (JFP1)

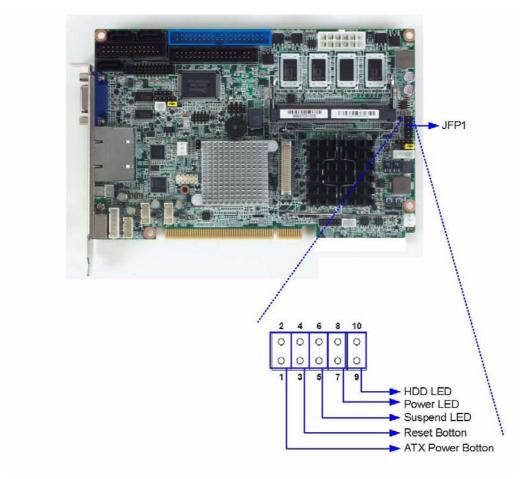


Figure 2.9 Front Panel Connectors (JFP1)

There are several external indicators and switches to help monitor and control the PCI-7031.

2.10.1 ATX Power Button (JFP1 Pin 1~2)

If your computer case is equipped with an ATX power supply, you should connect the power on/off button on your computer case to (JFP1 Pin 1~2). This connection enables you to turn your computer on and off.

2.10.2 Reset (JFP1 Pin 3~4)

Many computer cases offer the convenience of a reset button. Connect the wire for the reset button.

2.10.3 Suspend LED (JFP1 Pin 5~6)

You can connect an LED to connector (JFP1 Pin 5~6) to indicate when the system is in suspend status.

2.10.4 Power LED and keyboard lock connector (JFP1 Pin 7~8)

(JFP1 Pin 7~8) is a for the power on LED. Refer to Appendix B for detailed information on the pin assignments.

Table 2.1: ATX	power supply LED s	tatus (No support fo	r AT power)
Power mode	LED (ATX Power mode (On/off by tentative button)	e) LED (AT Power mode) (On/off by switch of Power supply)	LED (AT Power mode) (On/off by front panel Switch)
System On	On	On	On
System Suspend	Fast flashes	Fast flashes	Fast flashes
System Off	Slow flashes	Off	Off

2.10.5 HDD LED (JFP1 Pin 9~10)

You can connect an LED to connector (JFP1 Pin 9~10) to indicate when the HDD is active.

2.11 Watch Dog Timer (JWDT1) / Infrared (JIR1)

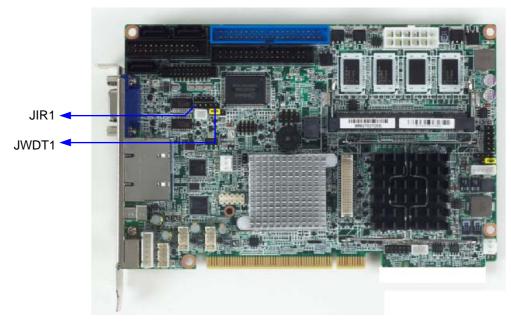


Figure 2.10 Watch Dog Timer (JWDT1) / Infrared (JIR1)

2.11.1 Watchdog timer output (JWDT1)

The PCI-7031 contains a watchdog timer that will reset the CPU in the event the CPU stops processing. This feature means the PCI-7031 will recover from a software failure or an EMI problem. The JWDT1 jumper settings control the outcome of what the computer will do in the event the watchdog timer is tripped.

Table 2.2: Watchdog timer output (JWDT1)			
Function	Jumper Setting		
GPIO14	1 2 3 O O O		
* System Reset	1 2 3 O O O 2 - 3 closed		

^{*} default setting

2.11.2 Infrared Connector (JIR1)

This 5-pin header is for connecting infrared device connector.

2.12 Dual Giga LAN RJ45 connector (LAN12)



Figure 2.11 Dual Giga LAN RJ45 connector (LAN12)

PCI-7031 uses the Intel[®] 82567V/82583V Gigabit LAN chips are linked to dedicated PCIe x1 lanes. PCI-7031 provide high throughputs for heavy loading networking environment. It provides two RJ-45 connectors in the rear side and is convenient for most industrial applications.

2.13 High Definition Audio Interface (HDAUD1)

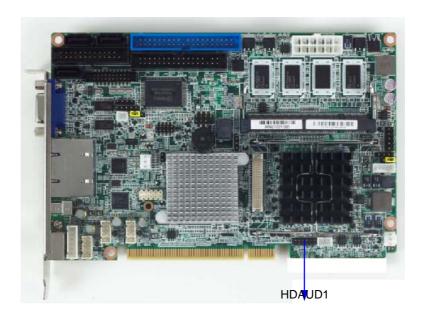


Figure 2.12 High Definition Audio Interface (HDAUD1)

The PCI-7031 provides high definition audio through PCA-AUDIO-HDA1E module.

2.14 Serial ATA interface (SATA1 ~ SATA3)

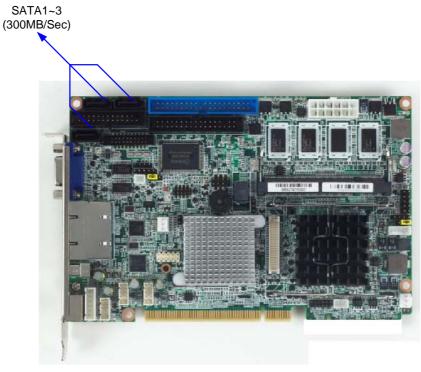


Figure 2.13 Serial ATA interface (SATA1 ~ SATA3)

In addition to the EIDE interface (up to two devices), the PCI-7031 features three high performance Serial ATA interfaces (up to 300 MB/s) for easy hard drive cabling with long, thin SATA cables.

2.15 LAN1 and LAN2 LED connector (LANLED1)

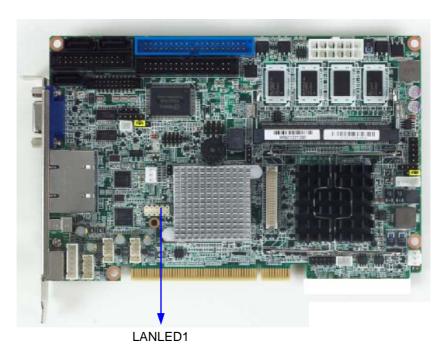


Figure 2.14 LAN1 and LAN2 LED connector (LANLED1)

PCI-7031 provides an external LAN LED pin header for connecting to the front side of the chassis. With this convenient design, users are alerted to LAN port activity. Refer to Appendix B for detailed information on the pin assignments.

2.16 GPIO header (GPIO1)

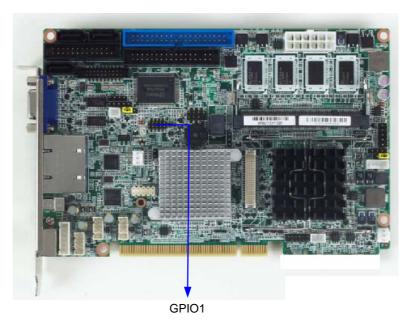


Figure 2.15 GPIO header (GPIO1)

PCI-7031 provides a 14-pin header for Digital I/O usage. Refer to Appendix B for detailed information on the pin assignments and programming guide in Appendix B.

2.17 CMOS clear (CMOS1)

The PCI-7031 single board computer contains a jumper that can erase CMOS data and reset the system BIOS information. Normally this jumper should be set with pins 1-2 closed. If you want to reset the CMOS data, set CMOS1 to 2-3 closed for just a few seconds, and then move the jumper back to 1-2 closed. This procedure will reset the CMOS to its default setting.

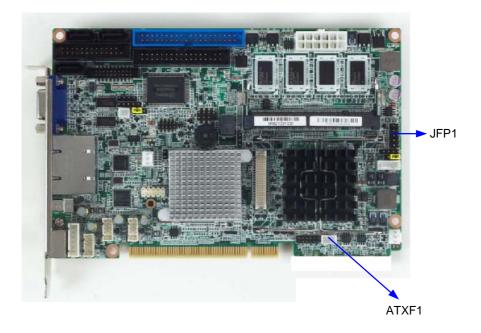
Table 2.3: CMOS (CMOS1)

Function	Jumper Setting
* Keep CMOS data	1 2 3 1 - 2 closed
Clear CMOS data	1 2 3 O O O 2 - 3 short

^{*} default setting



2.18 ATX Feature connector(ATXF1)



The PCI-703I can support an advanced soft power switch function. When using an ATX power supply, please follow the instructions below to enable ATX functions.

- 1. Find ATX feature cable (1700002343).
- 2. Connect the 3-pin plug of the cable to ATXF1 (ATX feature connector).
- 3. Connect the power on/off button cable of the chassis to JPF1's pins 9 and 10. Default value is set ATXF1 to short pin1-2.

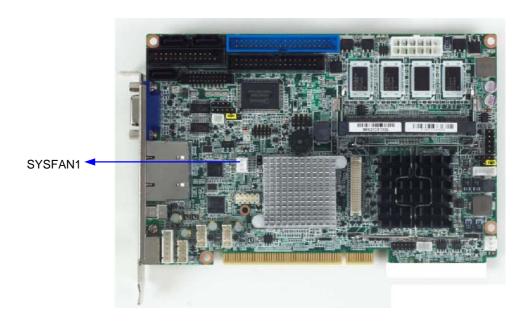
Important: Make sure that the ATX power supply can take at least a 10mA load on the 5 V standby lead (5 VSB). If not, you may have difficulty powering on your system.

2.19 ATX power control connector (ATX1)



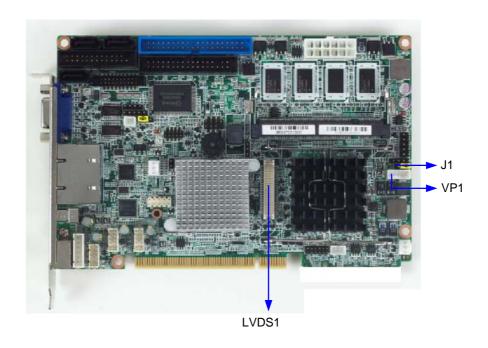
The PCI-7031 supports ATX power supply. ATX1 supplies main power (+5 V,+12 V, 5 VSB), and it is a 6 x 2 power connector.

2.20 System FAN connector (SYSFAN1)



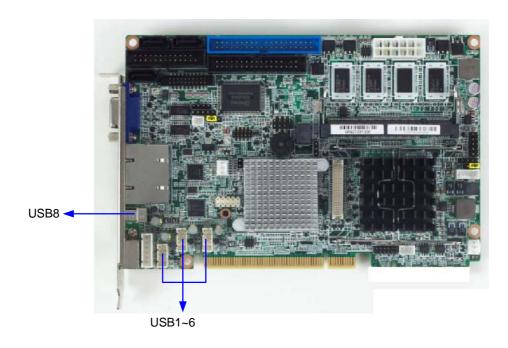
The PCI-7031 is equipped with a 3-pin FAN connector providing +12 V power for system FAN.

2.21 LVDS Signal and Power Connectors (LVDS1/VP1)



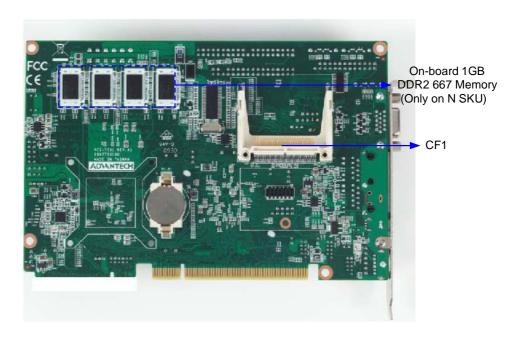
For PCI-7031, LVDS1 consists of a 40-pin connector which can support 18-bit single channel LVDS with resolution up to XGA (1024 x 768) & WXGA (1280 x 800). The LCD inverter is connected to VP1 via a 5-pin connector to provide power to the LCD display. J1 provides inverter voltage selection: close pins 1, 2 for 3.3V power input inverter; close pins 2, 3 for 5V power input inverter.

2.22 USB Ports (USB 1~6 & 8)



PCI-7031 supports 7 USB 2.0 ports, you may use the 1700008887 4-port USB cable kit to utilize any four of USB 1~6, USB 8 is located on the rear I/O bracket. USB 7 is reserved and can NOT be used.

2.23 CF Card Socket



PCI-7031 supports a CF card device, an installed CF card will occupy the master IDE device. Please locate it on the solder side of the CPU card.

2.24 Low Pin Count Device Connection Pin Header



PCI-7031 has a 14-pin female pin header on its solder side to support ÔUT ¼[c extension modules. You may purchase them to add 4 more RS-485 serial ports (COM ports) with auto flow control function. Please see ordering information below.

Part Number and Description:

PCA-COM485-00A1E: Four RS 422/485 COM module WITH auto flow control function.

Chapter

AMI BIOS Setup

AMI BIOS has been integrated into many motherboards, and has been very popular for over a decade. People sometimes refer to the AMI BIOS setup menu as BIOS, BIOS setup or CMOS setup.

With the AMI BIOS Setup program, you can modify BIOS settings and control the special features of your computer. The Setup program uses a number of menus for making changes and turning special features on or off. This chapter describes the basic navigation of the PCI-7031 setup screens.

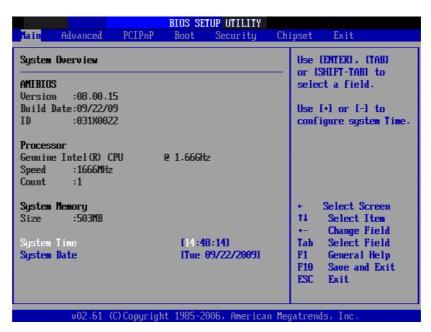


Figure 3.1 Setup Program Initial Screen

AMI's BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This information is stored in battery-backed up CMOS and it is retained when the power is turned off.

3.1 Entering Setup

Press the "Del" key during the Power On Self Test (POST) process to enter the BIOS setup screen, otherwise the system will continue the POST process.

3.2 Main Setup

When you first enter the BIOS Setup Utility, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the Main tab. There are two Main Setup options. They are described in this section. The Main BIOS Setup screen is shown below.

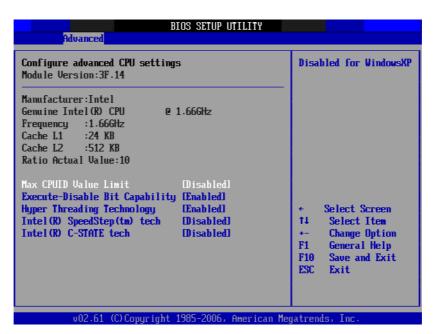


Figure 3.2 Main Setup Screen

The Main BIOS setup screen has two main frames. The left frame displays all the options that can be configured. Grayed-out options cannot be configured; options in blue can. The right frame displays the key legend.

Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it.

3.2.1 System time / System date

Use this option to change the system time and date. Highlight System Time or System Date using the <Arrow> keys. Enter new values through the keyboard. Press the <Tab> key or the <Arrow> keys to move between fields. The date must be entered in MM/DD/YY format. The time must be entered in HH:MM:SS format.

3.3 Advanced BIOS Features Setup

Select the Advanced tab from the PCI-7031 setup screen to enter the Advanced BIOS Setup screen. You can select any of the items in the left frame of the screen, such as CPU Configuration, to go to the sub menu for that item. You can display an Advanced BIOS Setup option by highlighting it using the <Arrow> keys. All Advanced BIOS Setup options are described in this section. The Advanced BIOS Setup screen is shown below. The sub menus are described on the following pages.



Figure 3.3 Advanced BIOS Features Setup Screen

3.3.1 CPU Configuration



Figure 3.4 CPU Configuration Settings

■ Max CPUID Value Limit

This is disabled for Windows XP.

Execute Disable Bit

This item specifies the Execute Disable Bit Feature. The settings are Enabled and Disabled. The Optimal and Fail-Safe default setting is Enabled. If Disabled is selected, the BIOS forces the XD feature flag to always return to 0.

Hyper-Threading Technology

While using a CPU with Hyper-Threading technology, you can select "Enabled" to enable Hyper-Threading Technology in an OS which supports Hyper-Threading Technology or select "Disabled" for other OSs which do not support Hyper-Threading technology.

■ Intel® SpeedStepTM tech

Intel SpeedStep Technology centralizes the control mechanism in the processor, eliminating the need for coordination with the chipset during the frequency/voltage configuration. This option is used to enable/disable the GV3 bit.

■ Intel® C-STATE tech

Intel® CPU Enhanced Halt (C1E) function, a function to save CPU power consumption in system halt state. When enabled, the CPU speed and voltage will be reduced during system halt state to save power consumption. You may choose to enable or disable it.

3.3.2 IDE Configuration

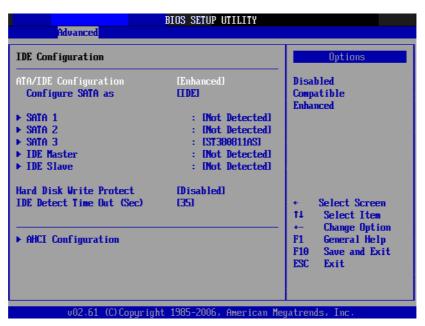


Figure 3.5 IDE Configuration

■ ATA/IDE Configuration

This can be configured as Disabled, Compatible or Enhanced.

Configure SATA as

This can be configured as IDE or AHCI.

■ SATA1/SATA2/SATA3

While entering setup, the BIOS automatically detects the presence of SATA devices. This displays the status of SATA device auto-detection.

IDE Master / Slave

While entering setup, the BIOS automatically detects the presence of IDE devices. This displays the status of IDE device auto-detection.

AHCI Configuration

AHCI is a new interface specification that allows the SATA controller driver to support advanced features. While entering setup, BIOS auto detects the presence of AHCI devices. This displays the status of auto detection of AHCI devices.

3.3.3 Super I/O Configuration



Figure 3.6 Super I/O Configuration

OnBoard Floppy Controller

Enable or disable the floppy function.

■ Floppy A

Select the type of floppy drive connected to the system. We suggest you disable the floppy if installing Windows Vista without a floppy drive.

Floppy B

Select the type of floppy drive connected to the system.

■ Floppy Mode Select

For user to set floppy mode, this must match specification of the floppy drive connected to CPU card, available options are 360 KB 5 1/4", 1.2 MB 5 1/4", 720 KB 3 1/2", 1.44 MB 3 1/2", 2.88 MB 3 1/2".

Serial Port1 Address

This option configures serial port 1 base addresses.

Serial Port2 Address

This option configures serial port 2 base addresses. The following options are also available:

Serial port2 Mode

This option configures serial port 2 mode. Available options include Normal, IrDA, ASK IR.

Parallel Port Address

This configures parallel port base addresses. The following options are also available:

Parallel Port Mode

This option configures Parallel Port mode. Available options include Normal, Bi-directional, ECP, EPP, ECP & EPP.

Parallel Port IRQ

This option configures s Parallel Port base IRQ.

Serial Port 3/4/5/6 Address

This option configures serial port 3/4/5/6 base addresses. The following options are also available:

Serial Port 3/4/5/6 IRQ
 This option configures serial port 3/4/5/63/4/5/63/4/5/63/4/5/6 base IRQ.

3.3.4 Hardware Health Function

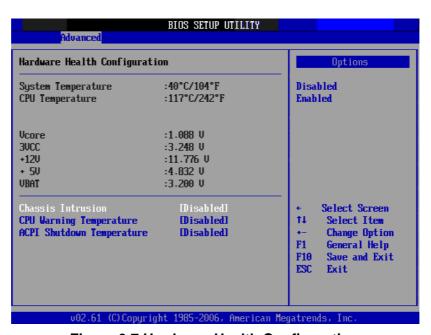


Figure 3.7 Hardware Health Configuration.

Hardware health function

Enable/Disable the onboard hardware monitor controller. If this option is enabled, the BIOS and OBS utility can get the system board's health information from hardware monitor controller.

Chassis Intrusion

Enable/Disable the Chassis Intrusion monitoring function. When the case is opened, the buzzer beeps.

CPU warning temperature

Use this to set the CPU warning temperature threshold. When the system reaches the warning temperature, the buzzer will beep.

ACPI Shut Down Temperature

This potion allows user to set the CPU temperature at that the system will automatically shut down for preventing CPU from over heat damage.

3.3.5 APM Configuration



Figure 3.8 APM Configuration

Power Management/APM

Enable or disable APM power management function.

Restore on AC Power Loss

This option allows user to set system action when AC power restores after AC power loss. Available options include Power Off, Power On, Last Status.

Resume On Ring

Disable/Enable RI wake event.

Resume On LAN

Disable/Enable LAN wake event.

Resume On PME

Disable/Enable PCIe device PME wake event.

Resume On RTC Alarm

Disable/Enable RTC wake event.

3.4 PCI/PNP Setup

Select the PCI/PnP tab from the PCI-7031 setup screen to enter the Plug and Play BIOS Setup screen. Highlighting a Plug and Play BIOS Setup option by using the <Arrow> keys displays a description in the righthand panel. All Plug and Play BIOS Setup options are described in this section. The Plug and Play BIOS Setup screen is shown below.

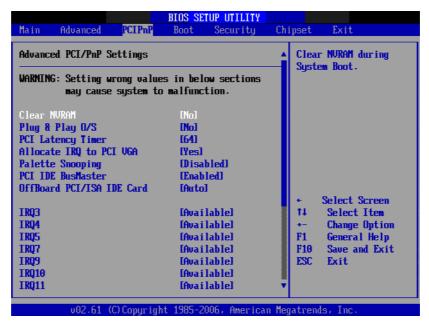


Figure 3.9 PCI/PNP Setup

Clear NVRAM

Set this value to force the BIOS to clear the Non-Volatile Random Access Memory (NVRAM). The Optimal and Fail-Safe default setting is No.

Plug and Play O/S

Set this value to allow the system to modify the settings for Plug and Play operating system support. The Optimal and Fail-Safe default setting is No.

■ PCI Latency Timer

Use this to adjust the PCI Latency Timer. This option sets the latency of all PCI devices on the PCI bus. The Optimal and Fail-Safe default setting is 64.

Allocate IRQ to PCI VGA

Set this value to allow or stop the system from giving the VGA adapter card an interrupt address. The Optimal and Fail-Safe default setting is Yes.

Palette Snooping

Set this value to allow the system to modify the Palette Snooping settings. The Optimal and Fail-Safe default setting is Enabled.

PCI IDE BusMaster

Set this value to allow or prevent the use of PCI IDE Busmastering. The Optimal and Fail-Safe default setting is enabled.

Off Board PCI/ISA IDE card

Set this value to allow an add-on PCI/ISA IDE card to be selected. The Optimal and Fail-Safe default setting is Auto.

IRQ

- IRQ[3,4,5,7,9,10,11,14,15]: Available: Specified IRQ is available to be used by PCI/PnP devices. Reserved: Specified IRQ is reserved for use by Legacy ISA devices. DMA Channel [0,1,3,5,6,7]:
- Available: Specified DMA is available to be used by PCI/PnP devices. Reserved: Specified DMA is reserved for use by legacy ISA devices. Reserved Memory Size: Size of memory block to reserve for legacy ISA devices.

3.5 **Boot Setup Utility**



Figure 3.10 Boot Settings Configuration

The following options are available:

Quick Boot

Allows the BIOS to skip certain tests while booting. This will decrease the time needed to boot the system.

Quiet Boot

If this option is set to Disabled, the BIOS displays normal POST messages. If Enabled, an OEM Logo is shown instead of POST messages.

AddOn ROM Display Mode

This is for choosing display mode of option ROM information under DOS environment during booting up process. Available options include Force BIOS, Keep Current.

Bootup Num-Lock

Select the Power-on state for Numlock.

PS/2 Mouse Support

Enable or disable PS/2 interface mouse support. Available options include Auto, Enable, Disable.

Wait For 'F1' If Error

Wait for the F1 key to be pressed if an error occurs.

- Hit 'DEL' Message Display
 - Displays "Press DEL to run Setup" in POST.
- Interrupt 19 Capture

Enable or disable option ROM to trap interrupt 19.

Bootsafe function

Enable or disable proprietary Bootsafe function.

3.6 Security Setup

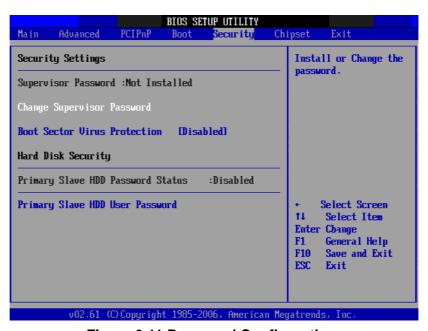


Figure 3.11 Password Configuration

Select Security Setup from the PCI-7031 Setup main BIOS setup menu. All Security Setup options, such as password protection and virus protection are described in this section. To access the sub menu for the following items, select the item and press <Enter>:

- Change Supervisor Password Provides for either installing or changing the password.
- **Boot sector Virus protection:** The boot sector virus protection will warn if any program tries to write to the boot sector.
- HDD Password Status

Allows user to set a password for accessing a specified HDD.

3.7 Advanced Chipset Settings



Figure 3.12 Advanced Chipset Settings

North Bridge Configuration

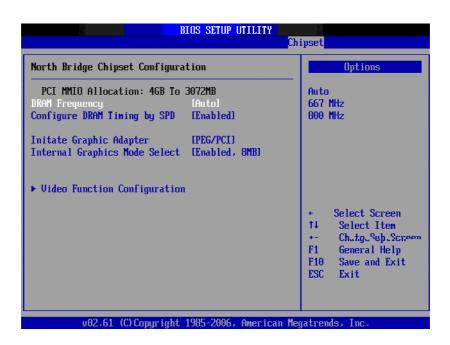
Allows user to set graphic and memory controller configurations.

South Bridge Configuration

Allows user to set I/O port configurations.

Spread Spectrum

Enable/Disable spread spectrum. Enable spread spectrum function can have better EMI compatibility but may cause some unexpected peripheral device incompatibility issue.





■ DRAM Frequency

Allows user to set DDR2 memory operating frequency.

■ Configure DRAM Timing by SPD

Allows user to set DRAM operating timing coefficients by SPD or Manual.

Initiate Graphic Adapter

Allows user to set initial video output device. Available options include IGD, PCI/IGD.

■ Internal Graphics Mode Select

Allows user to set graphic mode for DOS environment. Available options include Disable, Enable 4MB, Enable 8MB.

Video Function Configuration

This allows user to set IGD (Integrated Graphics Device) configuration.

■ DVMT model select

Displays the active system memory mode.

DVMT / FIXED Memory

Specify the amount of DVMT / FIXED system memory to allocate for video memory.

Flat Panel Type

Allows user to set LVDS panel resolution and signal width. This should match the specification of LVDS panel connected to the CPU card.

Spread Spectrum

Enable/Disable spread spectrum. Enable spread spectrum function can have better EMI compatibility but may cause some unexpected peripheral device incompatibility issue.

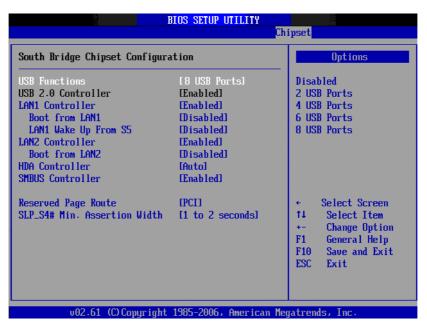


Figure 3.13 Souh Bridge Configuration

USB Functions

Select: Disabled, 2 USB Ports, 4 USB Ports, 6 USB Ports or 8 USB Ports.

USB 2.0 Controller

Enables or disables the USB 2.0 controller.

LAN 1/2 Controller

Enables or disables the LAN 1/2 GbE controller(s). The options below are also available.

Boot from LAN1/2

Allows user to enable or disable the function of LAN booting from a PXE server.

LAN1 Wake Up From S5:

Enables or disables LAN1 Wake Up From S5 function.

Boot from LAN 1/2:

Enables or disables GbE LAN 1/2 boot function.

HDA Controller

Enables or disables the High Definition audio controller.

SMBUS Controller

Enables or disables the SMBUS controller.

Reserved Page Route

Allows user to set Port 80 information output port. Available options include PCI, LPC.

SLP S4# Min. Assertion Width

This is for setting delay time between stand by power readiness and ICH SLP_S4# signal triggering. Available options include 1 to 2 seconds, 2 to 3 seconds, 3 to 4 seconds, 4 to 5 seconds.

3.8 Exit Options



Figure 3.14 Exit Options

3.8.1 Save Changes and Exit

When you have completed system configuration, select this option to save your changes, exit BIOS setup and reboot the computer so the new system configuration parameters can take effect.

- 1. Select Save Changes and Exit from the Exit menu and press <Enter>. The following message appears:
 - Save Configuration Changes and Exit Now? [Ok] [Cancel]
- 2. Select Ok or Cancel.

3.8.2 Discard Changes and Exit

Select this option to quit Setup without making any permanent changes to the system configuration.

- 1. Select Discard Changes and Exit from the Exit menu and press <Enter>. The following message appears:
 - Discard Changes and Exit Setup Now? [Ok] [Cancel]
- 2. Select Ok to discard changes and exit.

3.8.3 Discard Changes

3. Select Discard Changes from the Exit menu and press <Enter>.

3.8.4 Load Optimal Defaults

The PCI-7031 automatically configures all setup items to optimal settings when you select this option. Optimal Defaults are designed for maximum system performance, but may not work best for all computer applications. In particular, do not use the Optimal Defaults if your computer is experiencing system configuration problems. Select Load Optimal Defaults from the Exit menu and press <Enter>.

3.8.5 Load Failsafe Defaults

The PCI-7031 automatically configures all setup options to failsafe settings when you select this option. Failsafe Defaults are designed for maximum system stability, but not maximum performance. Select Failsafe Defaults if your computer is experiencing system configuration problems.

- Select Load Failsafe Defaults from the Exit menu and press <Enter>. The following message appears:
 Load Failsafe Defaults?
 [OK] [Cancel]
- 2. Select OK to load Failsafe defaults.

Chapter

ftwaro

Value-Added Software Services

4.1 Value-Added Software Services

Software API: An interface that defines the ways in which an application program may request services from libraries and/or operating systems. Provides not only the underlying drivers required but also a rich set of user-friendly, intelligent and integrated interfaces, which speeds development, enhances security and offers add-on value for applications. It plays the role of catalyst between developer and solution, and makes embedded platforms easier and simpler to adopt and operate with customer applications.

4.1.1 Software API

4.1.1.1 Control

GPIO



General Purpose Input/Output is a flexible parallel interface that allows a variety of custom connections. allows users to monitor the level of signal input or set the output status to switch on/off the device. Our API also provide Programmable GPIO, allows developers to dynamically set the GPIO input or output status.

SMBus



SMBus is the System Management Bus defined by Intel Corporation in 1995. It is used in personal computers and servers for low-speed system management communications. The SMBus API allows a developer to interface a embedded system environment and transfer serial messages using the SMBus protocols, allowing multiple simultaneous device control.

4.1.1.2 **Display**

Brightness Control



The Brightness Control API allows a developer to control brightness easily on an embedded device.

Backlight



The Backlight API allows a developer to control the backlight (screen) on/off on an embedded device.

4.1.1.3 **Monitor**

Watchdog



A watchdog timer (WDT) is a device that performs a specific operation after a certain period of time if something goes wrong and the system does not recover on its own. A watchdog timer can be programmed to perform a warm boot (restarting the system) after a certain number of seconds.

Hardware Monitor



The Hardware Monitor (HWM) API is a system health supervision API that inspects certain condition indexes, such as fan speed, temperature and voltage.

4.1.1.4 Power Saving

CPU Speed



Make use of Intel SpeedStep technology to reduce power consumption. The system will automatically adjust the CPU speed depending on the system loading.

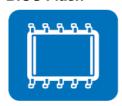
System Throttling



Refers to a series of methods for reducing power consumption in computers by lowering the clock frequency. These APIs allow the user to lower the clock from 87.5% to 12.5%.

4.1.2 Software Utility

BIOS Flash



The BIOS Flash utility allows customers to update the flash ROM BIOS version, or use it to back up current BIOS by copying it from the flash chip to a file on customers' disk. The BIOS Flash utility also provides a command line version and API for fast implementation into customized applications.

Embedded Security ID



The embedded application is the most important property of a system integrator. It contains valuable intellectual property, design knowledge and innovation, but it is easy to be copied! Embedded Security ID utility which provides reliable security functions for customers to secure their application data within embedded BIOS.

Monitoring



The Monitoring is a utility for customer to monitor the system health, like voltage, CPU and system temperature and fan speed. These items are important to a device, if the critical errors happen and not be solved immediately, a permanent damage may be caused.

Flash Lock



Flash Lock is a mechanism to bind the Board and CF card (SQFlash) together. User can "Lock" SQFlash via Flash Lock function and "Unlock" by BIOS while booting. A locked SQFlash cannot be read by any card reader or boot from other platforms without a BIOS with "Unlock" feature.

eSOS



The eSOS is a small OS stored in BIOS ROM. It will boot up in case of main OS crash. It will diagnose the hardware status, and then send an e-mail to administrator. The eSOS also provide Remote Connection: Telnet server and FTP server for administrator to rescue the system. Note: This function requires BIOS customization.

Chapter

Chipset Software Installation Utility

5.1 Before You Begin

To facilitate the installation of the enhanced display drivers and utility software, read the instructions in this chapter carefully. The drivers for the PCI-7031 are located on the software installation CD. The driver in the folder of the driver CD will guide and link you to the utilities and drivers under a Windows system. Updates are provided via Service Packs from Microsoft*.

Note!



The files on the software installation CD are compressed. Do not attempt to install the drivers by copying the files manually. You must use the supplied SETUP program to install the drivers.

Before you begin, it is important to note that most display drivers need to have the relevant software application already installed in the system prior to installing the enhanced display drivers. In addition, many of the installation procedures assume that you are familiar with both the relevant software applications and operating system commands. Review the relevant operating system commands and the pertinent sections of your application software's user manual before performing the installation.

5.2 Introduction

The Intel® Chipset Software Installation (CSI) utility installs the Windows INF files that outline to the operating system how the chipset components will be configured. This is needed for the proper functioning of the following features:

- Core PCI PnP services
- IDE Ultra ATA 100/66/33 and Serial ATA interface support
- USB 1.1/2.0 support (USB 2.0 driver needs to be installed separately for Win98)
- Identification of Intel® chipset components in the Device Manager
- Integrates superior video features. These include filtered sealing of 720 pixel DVD content, and MPEG-2 motion compensation for software DVD

5.3 Windows XP/XP Embedded/CE Driver Setup

 Insert the driver CD into your system's CD-ROM drive. You can see the driver folder items. Navigate to the "DRV_INF" folder and click "infinst_autol.exe" to complete the installation of the driver.

Note! Wrong driver installation may cause unexpected system instability.





Chapter

Integrated Graphic Device Setup

6.1 Introduction

To benefit from the Intel® Atom D510/N450 integrated graphics controller, you need to install the graphic driver.

6.2 Windows XP/XP Embedded/CE Driver Setup

Note!



Before installing this driver, make sure the CSI utility has been installed in your system. See Chapter 4 for information on installing the CSI utility.

Insert the driver CD into your system's CD-ROM drive. You can see the driver folders items. Navigate to the "DRV_VGA" folder and click "setup.exe" to complete the installation of the driver.

Note! Wrong driver installation may cause unexpected system instability.





Chapter

LAN Configuration

7.1 Introduction

The PCI-7031 has dual Gigabit Ethernet LANs via dedicated PCI Express x1 lanes (Intel 82567V (LAN1) and 82583V (LAN2)) that offer bandwidth of up to 500 MB/sec, eliminating the bottleneck of network data flow and incorporating Gigabit Ethernet at 1000 Mbps.

7.2 Installation

Note!



Before installing the LAN drivers, make sure the CSI utility has been installed on your system. See Chapter 4 for information on installing the CSI utility.

The PCI-7031's Intel 82567V (LAN1) and 82583V (LAN2) Gigabit integrated controllers support all major network operating systems. However, the installation procedure varies from system to system. Please find and use the section that provides the driver setup procedure for the operating system you are using.

7.3 Windows XP/XP Embedded/CE Driver Setup

Insert the driver CD into your system's CD-ROM drive. Navigate to the "DRV_LAN" folder and click "setup.exe" to complete the installation of the driver.

Note! Wrong driver installation may cause unexpected system instability.





Appendix A

Programming the Watchdog Timer

A.1 Watchdog Timer

The PCI-7031's watchdog timer can be used to monitor system software operation and take corrective action if the software fails to function after a programmed period. This section describes the operation of the watchdog timer and how to program it.

A.1.1 Watchdog Timer Overview

The watchdog timer is built into the super I/O controller W83627DHG-P. It provides the following functions for user programming:

- Can be enabled and disabled by user program.
- Timer can be set from 1 to 255 seconds or 1 to 255 minutes.
- Generates an interrupt or resets signal if the software fails to reset the timer after time-out.

A.1.2 Reset/ Interrupt Selection

The JWDT1 jumper is used to trigger system reset signal or to change GPIO14 state in the event the watchdog timer is tripped. See Chapter 1 for detailed jumper settings.

A.1.3 Programming the Watchdog Timer

The I/O port address of the watchdog timer is 2E(hex) and 2F(hex).

2E (hex) is the address port. 2F(hex) is the data port.

You must first assign the address of the register by writing an address value into address port 2E(hex), then write/read data to/from the assigned register through data port 2F (hex).

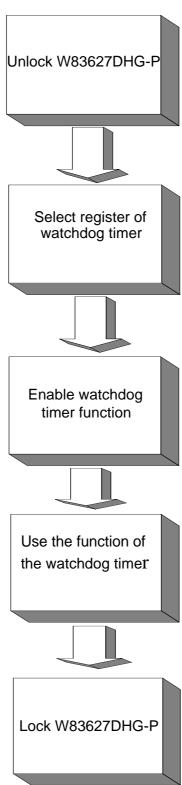


Table A.1: Watchdog Timer Registers				
Address of register (2E)	Attribute			
Read/Write	Value (2F) and description			
87 (hex)		Write this address to I/O address port 2E (hex) twice to unlock theW83627DHG-P		
07 (hex)	write	Write 08 (hex) to select register of watchdog timer.		
30 (hex)	write	Write 01 (hex) to enable the function of the watchdog timer. Disabled is set as default.		
F5 (hex)	write	Set seconds or minutes as units for the timer.		
Write 0 to bit 3: set second as counting unit. [default]				
Write 1 to bit 3: set minute as counting unit				
F6 (hex)	write	0: stop timer [default] 01~FF (hex): The amount of the count, in seconds or minutes, depends on the value set in register F5 (hex). This number decides how long the watchdog timer waits for strobe before generating an interrupt or reset signal. Writing a new value to this register can reset the timer to count with the new value.		
F7 (hex)	read/write	Bit 6: Write 1 to enable keyboard to reset the timer, 0 to disable.[default] Bit 5: Write 1 to generate a timeout signal immediately and automatically return to 0. [default=0] Bit 4: Read status of watchdog timer, 1 means timer is ""time out""."		
AA (hex)		Write this address to I/O port 2E (hex) to lock the watch-dog timer.2		

A.1.4 Example Program

Enable watchdog timer and set 10 sec. as timeout interval Mov dx,2e ; Unlock W83627DHG-P Mov al,87h Out dx,al Out dx,al Mov al,07h ; Select registers of watchdog timer Out dx,al Inc dx Mov al,08h Out dx,al Dec dx ; Enable the function of watchdog timer Mov al,30h Out dx,al Inc dx Mov al,01h Out dx,al Dec dx ; Set second as counting unit Mov al,0f5h Out dx,al Inc dx In al,dx And al, not 08h Out dx,al Dec dx ; Set timeout interval as 10 seconds and start counting Mov al,0f6h Out dx,al Inc dx Mov al,10 Out dx,al ; lock W83627DHG-P Dec dx Mov al,0aah Out dx,al 2. Enable watchdog timer and set 5 minutes as timeout interval Mov dx,2eh ; unlock W83627DHG-P Mov al,87h Out dx,al Out dx,al

:		
Mov al,0 Out Inc Mov Out	07h dx,al dx al,08h dx,al	; Select registers of watchdog timer
Dec dx Mov Out Inc Mov Out	al,30h dx,al dx al,01h dx,al	; Enable the function of watchdog timer
Dec dx Mov Out Inc In Or al,00	al,0f5h dx,al dx al,dx 8h dx,al	; Set minute as counting unit
Dec dx Mov Out Inc Mov Out	al,0f6h dx,al dx al,5 dx,al	; Set timeout interval as 5 minutes and start counting
Dec dx Mov Out 3.	al,0aah dx,al Enable wa	; lock W83627DHG-P
Mov dx, Mov al, Out dx, Out dx,	,2eh 87h al al	; unlock W83627DHG-P
Mov al, Out Inc Mov Out	07h dx,al dx al,08h dx,al	; Select registers of watchdog timer

```
Dec dx
                 ; Enable the function of watchdog timer
Mov
       al,30h
Out
       dx,al
Inc
       dx
Mov
       al,01h
Out
       dx,al
Dec dx
                ; Enable watchdog timer to be reset by mouse
Mov
       al,0f7h
Out
       dx,al
       dx
Inc
In
       al.dx
Or al,80h
Out
       dx,al
Dec dx
                ; lock W83627DHG-P
Mov
       al,0aah
Out
       dx,al
4.
       Enable watchdog timer to be reset by keyboard
_____
Mov dx,2eh ; unlock W83627DHG-P
Mov al,87h
Out dx,al
Out dx,al
Mov al,07h
               ; Select registers of watchdog timer
Out
       dx,al
Inc
       dx
Mov
       al,08h
Out
       dx,al
                ; Enable the function of watchdog timer
Dec dx
Mov
       al,30h
Out
       dx,al
Inc
       dx
Mov
       al,01h
Out
       dx,al
                ; Enable watchdog timer to be strobed reset by keyboard
Dec dx
Mov
       al,0f7h
Out
       dx,al
Inc
       dx
In
       al,dx
Or al,40h
Out
       dx,al
```

Dec dx ; lock W83627DHG-P Mov al,0aah Out dx,al 5. Generate a time-out signal without timer counting Mov dx,2eh ; unlock W83627DHG-P Mov al,87h Out dx,al Out dx,al ._____ Mov al,07h ; Select registers of watchdog timer Out dx,al Inc dx Mov al,08h Out dx,al Dec dx ; Enable the function of watchdog timer Mov al,30h Out dx,al Inc dx Mov al,01h Out dx,al Dec dx ; Generate a time-out signal Mov al,0f7h Out dx,al ;Write 1 to bit 5 of F7 register Inc dx In al,dx Or al,20h Out dx,al ; lock W83627DHG-P Dec dx

Mov

Out

al,0aah

dx,al

Appendix B

I/O Pin Assignments

B.1 Front Panel Connectors (JFP1)

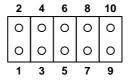


Table B.1: Front Panel Connectors (JFP1)				
Pin	Signal	Pin	Signal	
1	HDD LED+	2	HDD LED-	
3	Power LED+	4	Power LED-	
5	Suspend LED+	6	Suspend LED-	
7	System Reset Button	8	GND	
9	ATX Power Button	10	GND	

B.2 USB Ports (USB12/USB34/USB56)

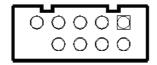


Table B.2: USB Ports (USB12/USB34)				
Pin	Signal	Pin	Signal	
1	VCC	2	VCC	
3	USB Data1-	4	USB Data2-	
5	USB Data1+	6	USB Data2+	
7	GND	8	GND	
9	GND	10		

B.3 IR Connector (JIR1)

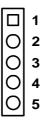


Table B.3: IR Connector (JIR1)		
Pin	Signal	
1	VCC	
2	NC	
3	IR_RX	
4	GND	
5	IR_TX	

B.4 Serial Ports (COM12)

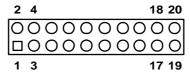


Table B.4: Serial Ports (COM12)				
Pin	Signal	Pin	Signal	
1	DCD1	2	DSR1	
3	RX1	4	RTS1	
5	TX1	6	CTS1	
7	DTR1	8	RI1	
9	GND	10	GND	
11	DCD2	12	DSR2	
13	RX2	14	RTS2	
15	TX2	16	CTS2	
17	DTR2	18	RI2	
19	GND	20	GND	

B.5 PS/2 Keyboard / Mouse connector (KBMS2)



Table B.5: PS/2 Keyboard / Mouse connector (KBMS2)			
Pin	Signal		
1	PS2 keyboard clock		
2	PS2 keyboard data		
3	PS2 mouse data		
4	GND		
5	VCC		
6	PS2 mouse clock		

B.6 LAN LED connector (LANLED1/LANLED2)

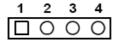


Table B.6: LAN LED connector (LANLED1/LANLED2)		
Pin	Signal	
1	LAN1_LINK/ACTIVITY#	
2	LAN1_1000#	
3	VCC3	
4	LAN1_100#	

B.7 ATX Feature connector(ATXF1)

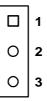


Table B.7: ATX Feature connector(ATXF1)		
Pin	Signal	
1	5V standby	
2	VCC	
3	PS_ON#	

B.8 CPU FAN connector (CPUFAN1)



Table B.8: CPU FAN connector (CPUFAN1)			
Pin	Signal		
1	FAN_PWM		
2	+12V		
3	FAN_TACH		

B.9 System FAN connector (SYSFAN1)



Table B.9: System FAN connector (SYSFAN1)		
Pin	Signal	
1	FAN_PWM	
2	+12V	
3	FAN_TACH	

B.10 Audio Interface Connector (HDAUD1)

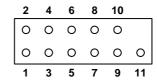


Table B	Table B.10: Audio Interface Connector (HDAUD1)				
Pin	Signal	Pin	Signal		
1	ACZ_VCC	2	GND		
3	ACZ_SYNC	4	ACZ_BITCLK		
5	ACZ_SDOUT	6	ACZ_SDIN0		
7	ACZ_SDIN1	8	ACZ_RST#		
9	ACZ_12V	10	GND		
11	GND	12			

B.11 GPIO Header (GPIO1)

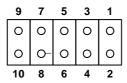


Table B.11: GPIO Header (GPIO1)				
Pin	Signal	Pin	Signal	
1	GPIO1	2	GPIO5	
3	GPIO2	4	GPIO6	
5	GPIO3	6	GPIO7	
7	GPIO4	8	GPIO8	
9	VCC	10	GND	

B.12 LVDS Connector (LVDS1)

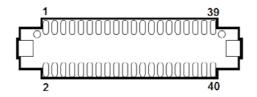


Table B.	12: LVDS Connector (LVDS1)	
Pin	Signal	Pin	Signal
1	LVDS_VCC	2	LVDS_VCC
3	GND	4	GND
5	LVDS_VCC	6	LVDS_VCC
7	LVDS0_D0-	8	LVDS1_D0-
9	LVDS0_D0+	10	LVDS1_D0+
11	GND	12	GND
13	LVDS0_D1-	14	LVDS1_D1-
15	LVDS0_D1+	16	LVDS1_D1+
17	GND	18	GND
19	LVDS0_D2-	20	LVDS1_D2-
21	LVDS0_D2+	22	LVDS1_D2+
23	GND	24	GND
25	LVDS0_CLK-	26	LVDS1_CLK-
27	LVDS0_CLK+	28	LVDS1_CLK+
29	GND	30	GND
31	LVDS0_DDC_SC	32	LVDS0_DDC_SD
33	GND	34	GND
35	NC	36	NC
37	NC	38	NC
39	NC	40	NC

B.13 LCD Inverter Connector (VP1)

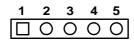


Table B.13: LCD Inverter Connector (VP1)		
Pin	Signal	
1	+12V	
2	GND	
3	BACK_ON#	
4	Brightness	
5	VCC	

B.14 SM Bus Connector (SMBUS1)

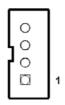


Table B.14: SM Bus Connector (SMBUS1)			
Pin	Signal		
1	VCC		
2	SMBUS CLK		
3	SMBUS Data		
4	GND		

B.15 Low Pin Count Header (LPC1)

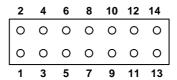


Table B.15: Low Pin Count Header (LPC1)				
Signal	Pin	Signal		
LPC_CLK	2	LPC_LAD1		
LPC_RST#	4	LPC_LAD0		
LPC_FRAME#	6	+3.3V		
LPC_LAD3	8	GND		
LPC_LAD2	10	NC		
SERIRQ	12	PWROK		
5V Standby	14	+5V		
	Signal LPC_CLK LPC_RST# LPC_FRAME# LPC_LAD3 LPC_LAD2 SERIRQ	Signal Pin LPC_CLK 2 LPC_RST# 4 LPC_FRAME# 6 LPC_LAD3 8 LPC_LAD2 10 SERIRQ 12		

B.16 ATX Power Control Connector (ATX1)

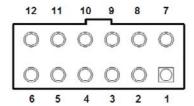


Table B.16: ATX Power Control Connector (ATX1)			
Pin	Signal	Pin	Signal
1	GND	7	GND
2	+5V	8	GND
3	+5V	9	5V Standby
4	GND	10	PSON#
5	+5V	11	GND
6	+5V	12	+12V

B.17 VGA Connector (VGA1)

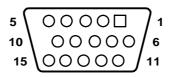


Table B.17: VGA Connector (VGA1)				
Pin	Signal	Pin	Signal	
1	RED	9	CRT_VCCIN	
2	VGA_G	10	GND	
3	VGA_B	11	N/C	
4	N/C	12	V_SDAT	
5	GND	13	H-SYNC	
6	GND	14	V-SYNC	
7	GND	15	V_SCLK	

Appendix C

Programming the GPIO

C.1 Supported GPIO Register

Bellow are detailed description of the GPIO addresses and programming sample.

C.1.1 GPIO Registers

CRF0 (GP10-GP17 I/O selection register. Default 0xFF)

When set to '1', the respective GPIO port is programmed as an input port.

When set to '0', the respective GPIO port is programmed as an output port.

CRF1 (GP10-GP17 data register. Default 0x00)

If a port is programmed to be an output port, then its respective bit can be read/written.

If a port is programmed to be an input port, then its respective bit can only be read.

CRF2 (GP10-GP17 inversion register. Default 0x00)

When set to '1', the incoming/outgoing port value is inverted.

When set to '0', the incoming/outgoing port value is the same as in data register.

Extended Function Index Registers (EFIRs)

The EFIRs are write-only registers with port address 2Eh or 4Eh on PC/AT systems.

Extended Function Data Registers(EFDRs)

the EFDRs are read/write registers with port address 2Fh or 4Fh on PC/AT systems.

C.1.2 GPIO Example Program-1

Enter the extended function mode, interruptible double-write MOV DX.4EH MOV AL,87H **OUT DX,AL OUT DX,AL** Configure logical device 7(GP10~GP17), configuration register CRF0,CRF1,CRF2 _____ MOV DX,4EH MOV AL,07H; point to Logical Device Number Reg. **OUT DX,AL** MOV DX,4FH MOV AL,07H; select logical device 7 OUT DX,AL; MOV DX,4EH MOV AL, FO **OUT DX,AL** MOV DX,4FH MOV AL,00H; 01:Input 00:output for GP10~GP17 **OUT DX,AL** MOV DX,4EH MOV AL, F2H; **OUT DX,AL** MOV DX,4FH MOV AL,00H ;Set GPIO is normal not inverter OUT DX,AL; MOV DX,4EH MOV AL, F1H **OUT DX,AL** MOV DX,4FH MOV AL,??H; Put the output value into AL **OUT DX,AL** Exit extended function mode | -----MOV DX,4EH MOV AL, AAH **OUT DX,AL**