MICROPAC HC16

HARDWARE REFERENCE MANUAL

for Revision 3 boards

MANUAL Revision 2.0

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DISCLAIMER

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FCC COMPLIANCE

EMAC's MICROPAC series of computers and accessories are classified as sub-assemblies per FCC CST bulletin, No. 62, May 1984. The bulletin states that sub-assemblies are not themselves subject to the FCC rules. Only the end product is directly subject to the rules.

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INTRODUCTION

The MICROPAC HC16 board (referred to hereafter as the HC16) uses the MC68HC16Z1 microprocessor. Many of the features of the MICROPAC HC16 are built into the microprocessor itself and some require trading of one feature to gain another. The standard features are as follows:

PLL clock system which can be programmed "on-the-fly" to various frequencies under 16.78 MHz.
System protection logic, watchdog timer, clock monitor, and bus monitor.
UART with multiprocessor capability, idle line detect and 7/8 data bits with parity or 8/9 data bits without parity.
Eight channel, 8/10 bit A/D with 8 automated modes. The 8 analog inputs can be also be read as an 8 bit input port.
Two 16 bit free running counters with prescaler.
Three input capture channels.
Four output compare channels.
One input capture/output compare channel.
One pulse accumulator/event counter input.
Two pulse width modulation outputs clocked by an internal or external clock.
One non-maskable and three maskable external interrupt inputs.
Serial EEPROM (1K words) for secure parameter storage.
Internal battery-backed 1024-Byte SRAM which can be re-mapped on 1K boundaries.
Two socketed battery-backed 32K SRAMs
Battery-backed real time clock which keeps seconds, minutes, hours, date, month, day of week, and year.
Four digital inputs, 8 high current outputs, and 12 programmable I/O lines
LCD Interface connects to a wide variety of OPTREX and compatible character displays, with backlight control capability.
Background debugging port for cross-platform software development and debugging.

Optional Features include:

256K and 1M of SRAM
64K, 128K, 256K, 512K and 1 M of Flash
Coprocessor with a buffered RS-232 serial port and a keypad decoder which can decode up to 16 keys.
Eight channels of 8 bit D/A.
Conversion of the standard serial port to RS-422/485.

POWER REQUIREMENTS

ST1
1 ❒ POWER
2 ❒ GROUND
3 ❒ RESET*

The HC16 can be powered by a 5 volt regulated supply or an 8 to 15 volt unregulated DC supply depending on the setting of JP8. Typical unloaded current draw is 200 mA. Power is connected to the HC16 through ST1pin 1 and ground is available on pin 2. The board may be reset by bringing ST1 pin 3 to ground momentarily.
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The two configurations of JP8 are shown below:

JP8 

Default position with regulator in-circuit. Apply 8 to 15 VDC to ST1 pin 1.

JP8 

Position with bypassed regulator. Apply only 5 V regulated DC to ST1 pin 1.

MEMORY MAP

RAM The SRAM sockets U6 and U10 may be populated by 32K, 128K or 512K RAMs. U10 is selected by accessing even numbered addresses and U6 by odd numbered addresses. JP3 (under socket U10) should be moved to the position appropriate to the the size of the memory, as follows:

```
A-128K and 512K devices
B-32K devices
```

1M RAM OPTION

When 512K devices are installed, the A19 pins on the RAM sockets become a consideration. The pins go low upon reset/power-up because they are driven by an inverter which is driven by the A19/CS6*/ PORTC.3 pin which defaults to the PORTC.3 function with a high output upon reset/power-up. The A19 function can be enabled after power-up by some initialization code but it is not recommended, especially when booting from RAM. This is due to the fact that the A19 function has an opposite polarity than the PORTC.3 function, and when enabled after booting from RAM, the interrupt vectors and all code that resides in the lower half of memory are mapped to the upper half. See the assembly language drivers for details.

EPROM/Flash Socket U14 accepts 64K x 16 and 256K x 16 EPROMs and 64K x 16 PEROM (Flash). The board may alternatively be ordered with a surface mount Flash. These devices are organized as 128Kx16,256Kx16 and 512Kx16.

1M FLASH OPTION

When the 512Kx16 Flash is installed, the upper/lower half of the Flash will be accessed using the A21/CS8*/PORTC.5 pin, which defaults to the PORTC.5 function with a high output upon reset/power-up and drives the most significant address line of the Flash through an invertor. The A21 function (which addresses as if it were A19) can be enabled after power-up by some initialization code but it is not recommended, especially when booting from Flash. This is due to the fact that the A21 function has an opposite polarity than the PORTC.5 function, and when enabled after booting from Flash, the interrupt vectors and all code that resides in the lower half of memory are mapped to the upper half. See the assembly language drivers for details.

JP1 SETTINGS for EPROM

64K x 16 EPROM (AT27C1024)

```
      o o o o o=o
JP1 A B C D E F
```

256K x 16 EPROM (AT27C4096)

```
      o=o o o o=o
JP1 A B C D E F
```

JP1 SETTINGS for Flash

Flash

```
      o o=o o=o o
JP1 A B C D E F
```

Flash write protect mode

```
      o o o o=o o
JP1 A B C D E F
```

JP 1 has no effect on the surface mounted flash option.

Due to the addressing scheme used with the Flash devices, you will need to refer to the assembly language drivers for assistance with in-circuit Flash programming.

BOOT MEMORY OPTIONS

On reset the CPU may boot out of nonvolatile external SRAM or out of EPROM/Flash. Of course, before resetting, the proper initialization code should reside in the selected boot memory.

BOOT FROM EPROM/FLASH

In this configuration CSBOOT selects EPROM/Flash and chip select 0, 1, 2 and 3 (CS0-3) select SRAM.

```
   o o=o o=o
JP2 A B C D E
```

BOOT FROM EXTERNAL RAM

In this configuration, CSBOOT and chip select 1, 2 and 3 (CS1-3) select SRAM and CS0 selects EPROM/Flash.

```
   o=o o=o o
JP2 A B C D E
```

SERIAL EEPROM

This non-volatile memory is not part of the memory map and is intended to be used to hold configuration information and other data that doesn't change often, since the device is rated for only 10,000 write cycles. The memory is organized as 64X16 bits and all access is done serially through the SPI port pins using them as port lines. Refer to the distribution disk for assembly language driver examples.

HARDWARE DESCRIPTION

COPROCESSOR

The optional coprocessor adds the following features to the Micropac HC16: an additional serial port with a buffer for input characters and output characters, a 4 by 4 keypad decoder and a 16 bit counter. All communication to it is through the SPI with the IRQ3* interrupt used as an attention signal to the 68HC16. Due to the complexity of the interface it is described in the assembly language drivers software.

When special custom features are needed on the Micropac HC16, many of these can be implemented on the coprocessor. EMAC can custom program the coprocessor's firmware for almost unlimited applications (please call for a cost estimate for your requirements). Some hardware features available for a custom programmed coprocessor are: two 16 bit counter/timers, a serial port which can be used in synchronous or asynchronous mode, up to 12 I/O lines, and an analog comparator.

KEYPAD INTERFACE

With a standard coprocessor installed, a connection made between an X and Y axis on this header will be debounced and decoded into 16 unique characters depending on the combination selected. Refer to the assembly language drivers included on the distribution disk for an example using the keypad interface.

KEYPAD HDR 8

1							9
❒	❒	❒	❒	❒	❒	❒	❒
(X4)	(X3)	(X2)	(X1)	(Y4)	(Y3)	(Y2)	(Y1)

DIGITAL TO ANALOG CONVERTER

The D/A converter has 8 channels of 8 bit resolution with 0 to 5 volt analog output range. The D/A is selected when CS4 is asserted low, and address lines A6 low and A7 high. The data on A2, 1, 0 will determine which of the eight channels will be written. Writing 00 hex causes 0V to be output and writing FF hex causes the full scale voltage selected by VR1 to be output (the factory default setting is 5V).

+Vin is the voltage that is applied to pin 1 of ST1 and Vcc is the 5V regulated supply.

D/A CONNECTOR HDR 5

20 19		A2, A1, A0
❒ ❒	DAC 8	1 1 1
❒ ❒	DAC 7	1 1 0
❒ ❒	DAC 6	1 0 1
❒ ❒	DAC 5	1 0 0
❒ ❒	Vcc	
❒ ❒	DAC 4	0 1 1
❒ ❒	DAC 3	0 1 0
❒ ❒	DAC 2	0 0 1
❒ ❒	DAC 1	0 0 0
❒ ❒	+Vin	
2 1		

All even numbered pins are digital ground.

LCD INTERFACE

The LCD interface allows controlling of OPTREX and compatible character LCD panels. The power for LED backlighting may be turned on by a high output on PORTC.6. The contrast level may be controlled by a fixed resistor on the MICROPAC or by a remote potentiometer. Since most LCD displays are too slow to keep up with the standard I/O access times, an external DSACK (wait state) generator is included on-board which will slow down accesses to the LCD, but the external DSACK option must be selected for the LCD chip select before it can have an affect. This is demonstrated in the distribution disk assembly language drivers.

LCD CONNECTOR HDR 9

1		2
VCC	❒ ❒	GND
RS	❒ ❒	CONTRAST
E	❒ ❒	R/W*
D7	❒ ❒	D8
D9	❒ ❒	D10
D11	❒ ❒	D12
D13	❒ ❒	D14
BACKLIGHT K	❒ ❒	BACKLIGHT A
15		16

DIGITAL I/O

In the diagram of HDR6 PGP.x represent port lines controlled by individual bits of data register PORTGP and data direction register DDRGP. PF.x port lines are controlled by PORTF, PFPAR and DDRF. On reset, PGP defaults as inputs and PF defaults as active low interrupt inputs. Writing to PFPAR will allow changing the individual lines of PF to general purpose I/O lines. The data direction of a port line can be changed to output by setting the corresponding bit in the port's data direction register (DDRF or DDRGP) to 1. When a data direction bit is set, the data present in the corresponding bit of the port's data register (PORTGP or PORTF) will be seen on the port line. These pins also have alternate functions that will not be discussed here.

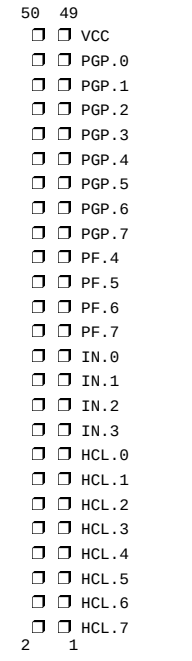
The IN.x lines are input (read) only and the port is accessed when CS4 and address lines A6 and A7 are asserted low. This input port is referred to in the assembly language drivers as INLATCH. IN.0 to IN.3 correspond directly to bits 0 to 3 of the port. Bits 4-6 of this port have pullups to Vcc and are available on JP7 for custom software jumper options or for general purpose inputs. Bit 7 is used as the handshake input detect from serial port COM1 (discussed later).

The HCL.x lines are high current output (write) only lines and the port is accessed when CS4 and A7 are low and A6 is high. This output port is referred to in the assembly language drivers as OUTPRT. At room temperature these lines are capable of sinking 500 mA per line with a package limit of 2.25 watts. If a bit is set in the data written to the port, the corresponding output will be sinking current. These port lines are not compatible with standard TTL logic (even if pullup resistors were added) because in the active state the voltage drop on the darlington pair output is around 0.9 V. On power on reset the outputs are inactive.

The following additional I/O lines are found on other headers but can be made available by configuring related registers and trading their primary functions (configuration registers not shown):

INPUTS:	PORTF.1	HDR 1 pin 18.
	PORTF.2	HDR 1 pin 16.
	(The above pins have invertors that invert the level before presenting them to PORTF, so this prevents them from also being used as outputs).	
	PORTADA	HDR 7 (see Analog Inputs section)
	PACTL.7	HDR 10 PIN 7 (Pulse accumulator pin state)
	PACTL.3	HDR 10 PIN 5 (PCLK pin state)
OUTPUTS:	PORTC.5	HDR 10 PIN 4
	PWMC.0	HDR 10 PIN 3 (PWM B)
	PWMC.1	HDR 10 PIN 1 (PWM A)
INPUT/OUTPUT:	PORTQS.1	HDR 11 PIN 1
	PORTF.3	HDR 11 PIN 3
	PORTF.0	HDR 10 PIN 2 (Understand the MODCLK function before using)

DIGITAL I/O HDR 6



All even numbered pins are digital ground.

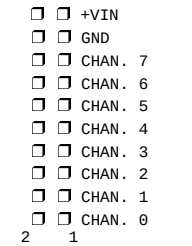
ANALOG INPUTS

The 8 channels of 8/10 bit A/D have a range of 0-5V. The upper end of this range is fine tuned when the unit is tested and may be adjusted using VR1 if it later gets out of calibration.

When 8 bit resolution is selected the accuracy is +-1 count; 10 bit resolution has an accuracy of +-2.5 counts. With a 16.78 MHz clock, a single 8 bit conversion will take 8 uS, and a single 10 bit conversion will take 9 uS.

Reading PORTADA will allow you to read the A/D lines as an 8 bit digital input port. The voltage present must be at the appropriate levels for an accurate digital reading. The ports may be used as analog and digital inputs simultaneously without reconfiguring.

Analog HDR 7



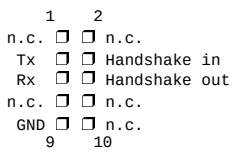
Pin 20 is a 10K pullup to Vcc and the rest of the even numbered pins and pin 17 are digital ground.

SERIAL PORTS

COM0

This serial port on HDR 3 is implemented using the optional coprocessor. The handshake output follows the level applied to the handshake input and cannot be controlled or monitored by software. Refer to the assembly language drivers included on the distribution disk for an example using this port.

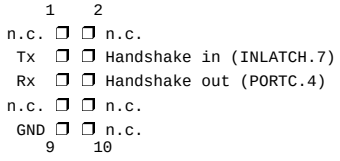
HDR 3 (COM0)
(RS-232 ONLY)



COM1

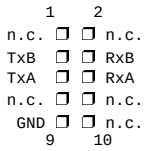
Serial port COM1 on HDR 2 is RS-232 in the standard configuration and has input and output handshake lines. The handshake input level can be detected by reading INLATCH bit 7 (described in the Digital I/O section). The handshake output can be controlled by PORTC.4 when the line has been configured as an I/O port.

HDR 2 (COM1)
(RS-232 CONFIGURATION)



This port may be factory configured as RS-422/485. This option allows up to 32 serial ports to share the same twisted pair. Each of them may take turns transmitting on the twisted pair by using PORTC.4 to selectively enable and disable their transmitters. A high on PORTC.4 enables the transmitter, and a low frees the twisted pair to be used by another transmitter. Each end of the pair should have a terminating resistor that matches the characteristic impedance of the line (typically 33 ohms can be used). The serial port allows for multiprocessor communication when the address mark wakeup function is enabled. This innovative function, when enabled, will interrupt the processor if the 8th bit (or 9th bit, if in 9 bit mode) of a data byte is set. Using the appropriate software allows for a powerful communication scheme.

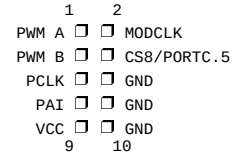
HDR 2 (COM1)
(RS-485 CONFIGURATION)



PWM HEADER

This makes available the pulse accumulator input, PWM A and PWM B outputs and the external clock drive (for the capture compare unit and for PWM A and PWM B). Also available on this header are MODCLK and CS8/PORTC.5 which are described in the Digital I/O section.

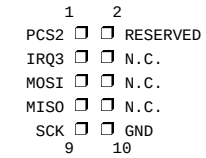
HDR 10



SPI HEADER

The serial peripheral interface (SPI) is available on HDR 11. This header is included on boards that don't have the coprocessor option. It includes all the pins necessary for SPI communication (MOSI, MISO and SCK), a peripheral chip select (PCS2) and an interrupt input (IRQ3). Note that MOSI is connected to MISO via a 1K resistor, so when one line is an input and the other an output, the input will follow the level of the output.

HDR 11



BACKGROUND DEBUGGING HEADER

This header allows connecting of the background debug cable (E400-00) for control and interrogation of the HC16 via a PC printer port.

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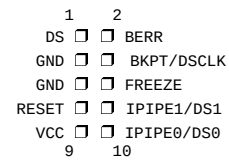
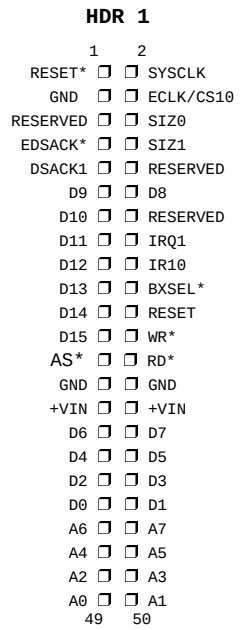
HDR 4



EXPANSION HEADER

This connector allows connection to EMAC peripherals, as well as peripherals of your own design. Included are:



D0-D15	16 bit data bus. When connecting to 8 bit peripherals, use only D8-D15.
A0-A7	the lower byte of the address bus.
BXSEL*	external I/O select line which is asserted low when CS4 is low and A6, A7 are high.
WR*	active low write select line.
RD*	active low read select line.
ECLK/CS10*	this defaults as CS10 but can be configured to provide ECLK (M6800 compatible bus clock).
SYSCLK	the clock output from the microprocessor.
RESET	active high RESET output
INT0, INT1	these are rising edge sensitive interrupt inputs which are connected through inverters to IRQ1 and IRQ2 respectively.
GND, +VIN	these provide ground and the voltage supplied to pin 1 of ST1.
Vcc	the system's 5 volt supply.

The following pins are new additions to the standard EMAC expansion header. These are not used on standard EMAC peripherals, and typically are not needed when interfacing to 8 bit peripherals.

EDSACK0*	this provides for dynamic bus sizing and asynchronous data transfers. This pin and the LCD wait state generator output are logically ANDed together and presented to the DSACK0 pin on the microprocessor.
DSACK1*	this provides for dynamic bus sizing and asynchronous data transfers.
SIZ0, SIZ1	these indicate the number of bytes to be transferred during a bus cycle.
AS*	this indicates that a valid address is on the address bus.

The reserved pins are not connected on this revision of the MICROPAC but may in future revisions, so to maintain compatibility they should be left unconnected in peripherals of your own design.

REAL TIME CLOCK

The real time clock (RTC) implemented using the Dallas Semiconductor DS1302. This device counts seconds, minutes, hours, day of the month, month, day of the week and year with leap year compensation. It also has 31 bytes of scratchpad RAM for parameter storage. Refer to the assembly language drivers included on the distribution disk for an example using the RTC.

The RTC is powered by an on-board 3V battery when power is off so time and scratchpad RAM are maintained. The battery is not rechargeable so do not enable the trickle charging function of the RTC, otherwise the battery will be damaged.

APPENDIX A

JUMPER DESCRIPTION

JP1 EPROM JUMPER SETTINGS

64K x 16 EPROM (AT27C1024)

256K x 16 EPROM (AT27C4096)

Flash JUMPER SETTINGS

64k x 16 Flash (AT29C1024)

Flash write protect mode

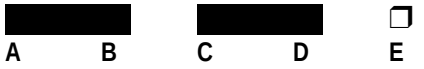
NOTE: JP1 has no effect on the surface mounted flash option.

JP2 BOOT MEMORY JUMPER SETTINGS

EPROM/Flash

In this configuration chip select 0, 1, 2 and 3 (CS0-3) select SRAM and CSBOOT selects EPROM/Flash

EXTERNAL RAM



In this configuration, chip select 0, 1, 2 and 3 (CS0-3) select EPROM/Flash and CSBOOT selects SRAM.

JP3 RAM SIZE JUMPER

JP3 in position A allows use of 128K and 512K devices and position B allows use of 32K devices.

JP4 INTERNAL RAM BATTERY BACKUP JUMPER

Position B allows battery backing of the RAM inside the 68HC16, position A powers the internal RAM with Vcc.

JP5 ON-BOARD RAM BATTERY BACKUP JUMPER

Position C enables the battery backing function for the RAM sockets. Position D disables this function.

JP7 SOFTWARE CONFIGURATION JUMPERS

These allow custom software to have jumper selectable options. Positions A, B and C correspond directly to bits 4, 5 and 6 of INLATCH (see Digital I/O section). When the jumpers are not populated, external pullups cause the bits to be read as highs. Putting a jumper in any position causes that bit to be read as a low.

JP8 5V REGULATOR JUMPER

Default position with regulator in-circuit. Apply 8 to 15 VDC to ST1 pin 1.

Position with bypassed regulator. Apply only 5 V regulated DC to ST1 pin 1.

APPENDIX B

MICROPAC HC16 Schematics