iPac 9302

User Manual

Revision 1.2
For use with Rev. 2.0 or greater iPac 9302.

EMAC, inc.
EQUIPMENT MONITOR AND CONTROL
2390 EMAC Way, Carbondale, IL 62902
World Wide Web: http://www.emacinc.com
(618) 529-4525 FAX: (618) 457-0110

Table of Contents

1. Introduction

This document describes EMAC's iPac 9302 Single Board Computer (SBC) module. The iPac 9302 is a PC/104 SBC sized module that provides a wide variety of I/O. Controlled by Cirrus' powerful EP9302 processor this module provides maximum flexibility with ample processing speed for most control applications. Although being extremely powerful with ample I/O for demanding applications, this board consumes minimal power, is low cost, and has a small footprint. The iPac 9302 uses the Standard PC/104 form factor (3.8" x 3.5") allowing the use of standard PC/104 mounting hardware and enclosures. The features of the iPac 9302 are as follows:

1.1 Features

- **CPU:** Cirrus Logic EP9302 ARM9 200 Mhz Processor with 100 Mhz System Bus, Floating Point Co-Processor and JTAG debugger capability.
- **MEMORY:** 8MB to 32MB of external on-board Flash in-circuit programmable, 256K bytes of EEPROM, and 8MB to 64MB of SDRAM.
- **DIGITAL I/O:** 16 General Purpose EP9302 Digital I/O lines, 16 CPLD Digital Inputs, 8 CPLD Digital Outputs, and 8 CPLD High Drive Digital Outputs.
- **PWM:** 1 EP9302 16-bit PWM and 2 CPLD 8-bit PWMs.
- **ANALOG INPUTS:** 5 channels of 12 bit A/D 0 – 3.3 volts.
- **ANALOG OUTPUTS:** 2 channels of 8 bit D/A using filtered PWM channels.
- **COMMUNICATION:** 1 RS232 Port and 1 RS232/422/485 port.
- **ETHERNET:** 1 10/100 BaseT Ethernet with RJ45.
- **USB:** 2 USB 2.0 Full-speed Host Ports.
- **TIME:** Battery-Backed Real-Time Clock/Calendar.
- **FLASH DISK:** MMC/SD hot-swap Flash Disk socket.
- **RESET:** External Reset Button provision.
- **INTERFACES:** EP9302 SPI, I2S, and AC97.
- **FORM FACTOR:** PC/104 Module with Dimensions of 96 mm x 90 mm (3.77" x 3.54").

1.2 On-Board Options

- **MEMORY:** Up to 32 MB of on-board Flash and 64 MB of SDRAM.
- **VIRTUAL I/O:** The CPLD can be reprogrammed to provide: Counters, Quadrature Decoders, SPI, Stepper Motor Controllers, and Keypad & LCD Interfaces.
- **SOFTWARE:** Linux, Windows CE, .NET Micro Framework.

1.3 Other Options

- PCD-39E00 Terminal Board**:** Screw Terminal Board allows for easy access to the iPac 9302 I/O. Up to two Screw Terminal Boards can be stacked onto a single iPac 9302.

2. Hardware

2.1 Specifications

- **VOLTAGE REQUIREMENTS:** 5 volt regulated +/- 5% DC board input voltage.
- **CURRENT REQUIREMENTS:** <500 ma. @ 5 Volts Typical (with no USB devices connected)
- **OPERATING TEMPERATURE:** 0 - 70 degrees Centigrade, humidity range without condensation 0% to 90% RH. Optional -40 – 80C temperature range.
- **DIGITAL I/O:** 16 programmable, EP9302 based, General Purpose TTL level I/O lines that can be configured as inputs or outputs. When configured as inputs a 3.3 volt high input voltage is to be used and when configured as outputs, they have a sink/source drive capability of 5 mA. 8 CPLD based digital outputs have a sink/source output drive capability of 25 mA. 16 digital inputs have 5 volt tolerant inputs. 8 open collector High-Drive Digital outputs with 500 mA. sink drive capability and a maximum total I/O drive of 1500 mA. for these 8 lines. All Digital I/O lines terminate to standard 50 pin, I/O Rack compatible header connectors.
- **ANALOG INPUTS:** 5 analog inputs are multiplexed into a 12-bit A/D converters with Sample & Hold and a conversion time of 1 mS. An additional 2 mS. of settling time may be required when switching between channels. The analog input voltage range for each channel is 0 – 3.3 Volts.

2.2 CPLD

A CPLD is located in the memory map within the physical address range of 0x00010000 to 0x0FFFFFFF. Though the iPac 9302 ships with the CPLD preprogrammed with a standard core, the CPLD is many-time programmable so it is possible to reprogram a new IP core for special applications. See the Custom Cores section for more information.

2.2.1 iPac 9302 A4 Core

The standard iPac 9302 A4 core contains 16, 8-bit registers which wrap over and over throughout the CPLD memory range. The 16 registers are shown in the table below.

ADDRESS	REGISTER NAME	TYPE
0x00010000	portw	gpi
0x00010001	portx	gpo
0x00010002	porty	gpo
0x00010003	portz	gpi
0x00010004	gpwma	pwmd
0x00010005	gpwmb	pwmd
0x00010006	status	gpi
0x00010007	control	gpo
0x00010008 0x00010009 : 0x0001000E	(not defined)	ugpi
0x0001000F	core_id	gpi

The register types are as follow:

REGISTER TYPE	DESCRIPTION
gpi	Input port. This is a read-only register.
gpo	Output port. This is a write-only register*.
pwmd	This is a write-only register*.
ugpi	This is an undefined gpi register*.

*Reading this type of register produces undefined results.

2.2.1.1 portx, porty

These are write-only output ports. Reading them produces undefined results. They output a max of 3.3V and the max current drive per pin is 25 mA. Note that on the iPac 9302, portx connects to a driver chip which increases its current sinking capability but the driver chip is only able to source current by pull-up resistors). See HDR1: CPLD-Based General Purpose Digital I/O.

2.2.1.2 portw, portz

These are read-only input ports. The input voltage should not exceed 5.0 Vdc or go below ground. Even though the CPLD's input lines are 5 volt tolerant, they are in fact 3.3 voltage level inputs and as such return a logic '1' for any voltage above 1.65 volts (half of the 3.3V Vdd).

2.2.1.3 gpwma, gpwmb

The 8-bit write-only registers, gpwma and gpwmb define the duty cycle for output pins PLD_PWM2 and PLD_PWM3, respectively. Control bits PIa or PIb (discussed later) if set to 1 invert the polarity of PLD_PWM2 and PLD_PWM3, respectively.

The CPLD gets its PWM base clock frequency from the processor's EGPIO[14]/PWMOUT1 pin. This clock signal decrements an 8-bit rollover counter within the CPLD which is compared against the values stored in gpwma and gpwmb to determine the respective outputs on PLD_PWM2 and PLD_PWM3 (see HDR2: Analog Channels & PWMs). Following is the PWM output truth table:

	PI*x*=0	PI*x*=1
counter >= gpwm*x*	0	1
counter < gpwm*x*	1	0

With a PIx bit set to 1, the respective gpwm*x* port sets the duty cycle according to the following formula:

$$DC = gpwm_x / 256$$

With a PIx bit set to 0, the respective gpwm*x* port sets the duty cycle according to the following formula:

$$DC = 100-(gpwm_x / 256).$$

For example, with the PIa bit set to 1, the duty cycle of a gpwma value of 0x00 gives a 0% duty cycle, and a value of 0xff gives a 99.6% duty cycle.

2.2.2 Status

This is a read-only register that returns various status bits.

7	6	5	4	3	2	1	0
-	-	-	-	-	CTS1	WP	CD

CD: SD/MMC card detect signal.

WP: SD/MMC write protect signal.
CTS1: COM1 Clear-To-Send signal.
"-" indicates unused/undefined bits.

2.2.3 control

This is a write-only register that allows the manipulation of several output bits.

7	6	5	4	3	2	1	0	
RTS1	PIb	PIa	-	-	PIO3	PIO2	PIO1	
0	0	0	0	0	0	0	0	RESET

PIO1,
PIO2,
PIO3: These control output pins PLDIO_01, 02, 03 respectively. Note that PLDIO_00 has no control provision in this core. See HDR2: Analog Channels & PWMs.

PIa,
PIb: These control the polarity of the gpwma and gpwmb outputs, respectively.

RTS1: COM1 Request-To-Send signal.

2.2.4 core_id

This read-only register returns the identification byte for the core. This is used to determine the type of core programmed into the CPLD. Returns 0xA4 for the A4 core.

2.2.5 Linux drivers

The iPac 9302 machine specific code of the EMAC patched Linux kernel creates a virtual mapping, reads the core_id register and classifies any devices created by the CPLD in the sysfs filesystem, providing user space access. Kernel patches are currently available through EMAC.

2.2.6 Custom Cores

While there is provision to reprogram the CPLD in-circuit, doing so will void your warranty. It is not a recommended practice since incorrect logic can damage the iPac 9302. Please contact EMAC for contract engineering and consulting services to design a custom or semi-custom CPLD core.

If you choose to void your warranty, Altera offers powerful free tools for programming the Max II plus. These tools include free and flexible modules for implementing UARTs, I2C, Counters, RAM, etc.
https://www.altera.com/support/software/download/altera_design/quartus_we/dnl-quartus_we.jsp

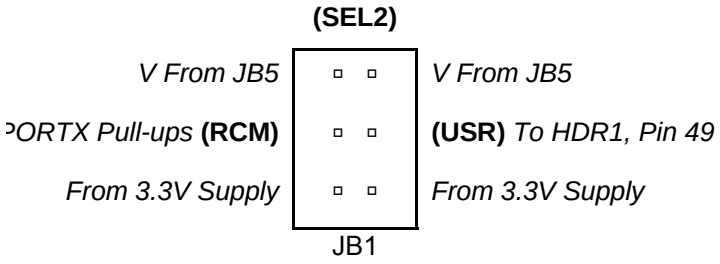
2.3 Jumpers

This section describes the Jumpers and Jumper Blocks of the iPac 9302.

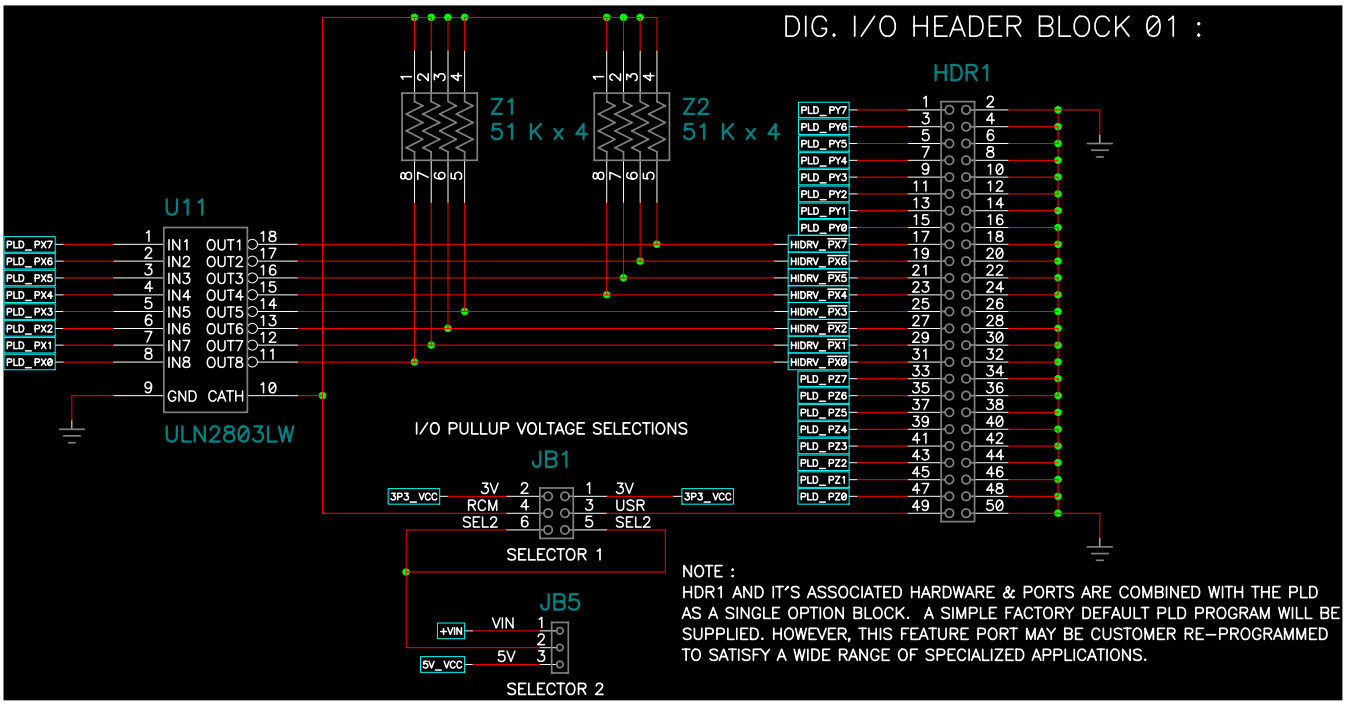
2.3.1 JB1

Pull-up Voltage. I/O Header (HDR1, pin 49) Voltage Selection & High Drive Pull-up Selection Jumper. See schematic below for the jumper block pin numbers.

.



JB1 controls the pull-up voltage of the High Drive Output lines and determines what voltage is present on pin 49 of HDR1. One side of the jumper (USR) controls pin 49 and the other side (RCM) controls the pull-up voltage of Port X. Leaving the USR shunt off leaves pin 49 open and leaving the RCM shunt off sets the High Drive Outputs to no pull-up voltage (open collector). The voltage at the SEL2 pins is defined by JB5.



2.3.2 JP2

Serial Select UART 1 (HDR5) Serial RS Selection Jumper.
(Note: on Rev0 PCBs the 232 & 485 PC Board labels are reversed)

Jumper	1	&	2	RS232 Serial
Jumper	3	&	4	RS422 Full Duplex (transmitter always on).
Jumper	5	&	6	RS485 (transmitter controlled by EGPIO[9]/485_~TXEN)

2.3.3 JB3

HDR3 Voltage. I/O Header (HDR3, pin 49) Voltage Selection Jumper.

Jumper	1	&	2	+3.3 volts applied to pin 49.
Jumper	2	&	3	+5 volts applied to pin 49.

2.3.4 JB4

Boot Select. Select normal or serial Boot option Jumper.

Jumper	1	&	2	Serial Boot through UART 1. See Boot ROM section of User's Guide.
Jumper	2	&	3	Normal Boot from Flash.

2.3.5 JB5

HDR1 Voltage. Select normal or serial Boot option Jumper.

Jumper	1	&	2	Vin (HDR4 Pin-4) provided to JB1.
Jumper	2	&	3	+5V provided to JB1.

2.4 Status LEDs

LD1 MMC/SD Flash Card access Red LED.

LD2 Ethernet Green LED Tree. Top LED is Link and bottom is Activity.

LD3 General Purpose Red Status LED controlled by processor pin RDLED. This may not be populated on some boards and in general its use is not recommended . This is because the output of this line is used as part of a workaround for a Cirrus EP9315A bug related to power-on reset. Since it is used in the reset workaround, asserting LD3 too long can reset the board.

LD4 General Purpose Green Status LED controlled by processor pin GRLED.

2.5 PB1: Button

PB1 Right Angle Processor Reset button.

2.6 HDR7: JTAG

This multipurpose header (HDR7) provides a programming interface to the CPLD which translates the bus signals as well as a JTAG debugging interface directly to the Processor. EMAC sells an adapter board (PER-ADP_00020) that provides a standard 10 pin Altera CPLD header and a standard 20 pin JTAG header. HDR7's pinout is a derivation of the standard 14 pin ARM JTAG header. EMAC has utilized several of the no-connect pins on this header to connect the CPLD JTAG connections. Debuggers such as Abatron's BDI series should be able to plug directly to this 14 pin header without the need for an adapter. EMAC is an authorized reseller of Abatron's BDI series of JTAG Debuggers. If you are interested in a JTAG debugger please contact EMAC for further information.

Table 1: JTAG & BDM Interface (HDR10)

Pin	Signal	Pin	Signal
1	3.3 Volts	2	GND
3	ARM_JTAG_Reset	4	GND
5	ARM_JTAG_TDI	6	PLD_JTAG_TDI
7	ARM_JTAG_TMS	8	PLD_JTAG_TMS
9	ARM_JTAG_TCK	10	PLD_JTAG_TCK
11	ARM_JTAG_TDO	12	Optional ARM Reset
13	NC	14	PLD_JTAG_TDO

2.7 HDR3: Processor-Based General-Purpose Digital I/O

These GPIO lines are for the most part exactly that, general purpose. Of these lines, 16 are connected directly to the processor (so use caution when interfacing to these lines) and 8 (Port W) are provided via the CPLD. The CPLD lines are by default programmed as inputs. The names of each line listed in Table 2 matches the port line on the EP9302 processor.

When using these processor lines as outputs these lines can drive 5 mA. and when used as inputs the input voltage should not exceed 3.3 Vdc or go below ground. Besides being bit configurable I/O lines they can also be used in variety of other functions as defined by these multiuse processor pins. See the EP9301 User's Manual for details.

When using the 8 input CPLD lines, the input voltage should not exceed 5.0 Vdc or go below ground. Even though the CPLD's input lines are 5 volt tolerant, they are in fact 3.3 voltage level inputs and as such define a high as any voltage above 1.65 volts (1/2 Vdd). Note: The CPLD can be reprogrammed to provide other functionality; see Custom Cores.

Table 2: PROCESSOR BASED DIGITAL I/O Connector (HDR3)

Pin	Signal	Pin	Signal
1	HGPIO[2]	2	GND
3	HGPIO[3]	4	GND
5	HGPIO[4]	6	GND
7	HGPIO[5]	8	GND
9	FGPIO[1]	10	GND
11	CGPIO[0]	12	GND
13	EGPIO[1]/CLK_1HZ	14	GND
15	EGPIO[2]	16	GND
17	EGPIO[3]/HDLCLK1	18	GND
19	EGPIO[6]/I2S-SDO2	20	GND
21	EGPIO[10]DREQ1	22	GND
23	EGPIO[11]/DACK1	24	GND
25	EGPIO[12]/DEOT1	26	GND
27	EGPIO[13]/I2S-SDI2	28	GND
29	EGPIO[14]PWMOUT1	30	GND
31	EGPIO[15]DASP	32	GND
33	PW0	34	GND
35	PW1	36	GND
37	PW2	38	GND
39	PW3	40	GND
41	PW4	42	GND
43	PW5	44	GND
45	PW6	46	GND
47	PW7	48	GND
49	3.3/5V (JB3)	50	GND

2.8 HDR1: CPLD-Based General Purpose Digital I/O

These input and output lines provide connections for heavier industrial relays and switches. They are connected to the CPLD of the iPac. There are 24 port lines in all and are broken up into three 8 bit ports (X, Y, & Z). Port X and Y are programmed as output ports and Z is an input port.

When using input Port Z, the input voltage should not exceed 5.0 Vdc or go below ground. Even though the CPLD's input lines are 5 volt tolerant, they are in fact 3.3 voltage level inputs and as such define a high as any voltage above 1.65 volts (half of the 3.3V Vdd).

The high-drive output port PX0 – PX7 has an open-collector output driver chip (ULN2803) with 500 mA. sink drive capability per line and a maximum total package current of 1500 mA. The open-collector output lines can source current by pull-up resistors to various levels selectable by Jumper JB1. The flyback diodes in the ULN2803 will be tied to the same voltage selected by JB1. Output Port Y port lines can drive up to 25 mA. loads.

Table 3: CPLD BASED DIGITAL I/O Connector (HDR1)

Pin	Signal	Pin	Signal
1	PY7	2	GND
3	PY6	4	GND
5	PY5	6	GND
7	PY4	8	GND
9	PY3	10	GND
11	PY2	12	GND
13	PY1	14	GND
15	PY0	16	GND
17	PX7	18	GND
19	PX6	20	GND
21	PX5	22	GND
23	PX4	24	GND
25	PX3	26	GND
27	PX2	28	GND
29	PX1	30	GND
31	PX0	32	GND
33	PZ7	34	GND
35	PZ6	36	GND
37	PZ5	38	GND
39	PZ4	40	GND
41	PZ3	42	GND
43	PZ2	44	GND
45	PZ1	46	GND
47	PZ0	48	GND
49	(see JB1 options)	50	GND

2.9 HDR2: Analog Channels & PWMs

The EP9302 processor on the iPac 9302 has a 12 bit, 5 channel A/D module which provides lines ANI0 – ANI4. These lines can accept signals in the range of 0 to 3.3 Volts.

In addition to the A/D, the iPac EP9302 provides 3 PWM channels which drive at 3.3V. One of the channels, EGPIO[14]/PWMOUT1, which is provided by the processor, is a 16-bit PWM with quite a bit of flexibility and has 5 mA drive capability (see EP9302 User's Guide for additional information). The other two PWMs, PLD_PWM2 & PLD_PWM3, are implemented within the CPLD and as such can drive up to 25 mA. loads. The clock source for PLD_PWM2 & PLD_PWM3 comes from EGPIO[14]/PWMOUT1 allowing the frequency for PWM2 & PLD_PWM3 to be programmable. Therefore, using EGPIO[14]/PWMOUT1 as a PWM output could in some cases prevent it from being an effective clock for PWM2 & PWM3, so most applications will either use the PWMOUT1 output for PWM, or use the PLD_PWM2 & PLD_PWM3 outputs for PWM but typically not all three at the same time. See gpwma, gpwmb.

In addition to the A/D and PWMs on HDR2, there are a number of processor specific I/O lines such as SPI, I2S, Interrupts, etc. as well as 4 CPLD lines (see control). Note: some of these processor lines are shared on HDR3.

Table 4: ANALOG (HDR2)

Pin	Signal	Pin	Signal
1	ANI0	2	ANI1
3	ANI2	4	ANI3
5	ANI4	6	GND
7	GND	8	GND
9	INTR1	10	INTR3
11	PLDIO_00	12	PLDIO_01
13	PLDIO_02	14	PLDIO_03
15	PLD_PWM2	16	PLD_PWM3
17	GND	18	GND
19	EGPIO[13]/I2S-SDI2	20	EGPIO[14]/PWMOUT1
21	GND	22	GND
23	SCLK1	24	SFRM1
25	SSPTX1	26	SSPRX1
27	GND	28	GND
29	ABTCK	30	ASYNC
31	ASDO	32	ASDI
33	ARSTN	34	EPGIO[4]/I2S-SDO1
35	EPGIO[5]/I2S-SDI1	36	EPGIO[6]/I2S-SDO2
37	GND	38	GND
39	5 Volts	40	3.3 Volts

2.10 HDR6: RS232 SERIAL UART0

The iPac 9302 provides one dedicated RS232 UART0 serial port which has software configurable baud rates. Both transmission and asynchronous data reception are possible. Handshake Lines are implemented by the use of the processors dedicated UART0 handshake lines.

Table 5: RS232 (HDR6)

Pin	Signal
1	DCD
2	DSR
3	RxD
4	RTS
5	TxD
6	CTS
7	DTR
8	RI
9	GND
10	NC

2.11 HDR5: RS232/422/485 SERIAL UART1

The iPac9302 provides one jumper (JB2) selectable RS232/422/485 UART which has software configurable baud rates. Both transmission and asynchronous data reception are possible. RS232 Handshake Lines (CTS & RTS) can be implemented by the programming of two CPLD lines (these lines are not programmed by default). When using this serial port in the RS422/485 mode, Processor Line EPGIO[9]/485_~TXEN controls the transmitter enable line of the RS422/485 driver. This can be done manually in software or automatically through a built-in provision in the hardware. Note: on rev0 PCBs the 232 & 485 silkscreen labels are reversed.

Table 6: RS485 (HDR5)

Pin	Signal
1	RS422/485 TX-
2	NC
3	RS232 RXD or 422/485 TX+
4	RTS (SPR_STATOUT)
5	RS232 TXD or 422/485 RX+
6	CTS (SPR_STATIN)
7	RS422/485 RX-
8	NC
9	GND
10	NC

2.12 HDR4: Alternate Power Connector

The iPac 9302 provides a keyed locking alternate power connector that lends itself more to industrial applications. This connector is the same as the power connector used on Floppy disk drives and shares the same pin-out. Therefore, a standard PC power supply can be used, provided it is loaded properly (some PC power supplies will not work unless the current drawn from the 5V line surpasses a predefined minimum). Pin #4 of HDR4 is referred to as Vin. This pin is routed exclusively to JB5 pin #1 as a jumper option. There is also a standard barrel type power jack (JK3, 2.1mm x 5.5mm x 9.5mm, Center Positive) that can be used to provide 5 volt regulated power.

Table 7: ALTERNATE POWER CONNECTOR (HDR4)

Pin	Description
1	+5 Volt Regulated
2	GND
3	GND
4	Vin*

* This pin is routed exclusively to JB5 pin #1 as a jumper option.

2.13 JK1: Ethernet

The iPac 9302 comes equipped with a 10/100 BaseT Ethernet port terminated to a standard RJ45 jack. In addition, a two LED tree is provided where the top LED is Link and the bottom is Activity. The iPac 9302 can be connected directly (point to point) to a PC with the use of a crossover Ethernet cable. To connect the iPac 9302 to a switch or a hub use a standard Ethernet cable.

The Ethernet MAC is provided internally within the processor (for programming details see the EP9301 User's Guide). The PHY is external to the processor and is implemented using a Intel LXT972 PHY chip. The PHY is a relatively power hungry chip and as such can be powered down in order to conserve power. Processor pin EGPIO[6]/I2S-SD02 can be optionally connected to the PWRDWN pin of the PHY by populating a 0 ohm resistor at location JR2. Contact EMAC if you need this feature.

2.14 JK2: USB

The iPac 9302 provides two USB 2.0 full-speed (12 Mbits/Sec.) Host ports. These ports are also capable of low-speed (1.5 Mbits/sec.) but are not Hi-Speed (480 Mbits/Sec.) capable. They are backwards compatible with USB 1.1 devices. USB devices (printer, mouse, keyboard, camera, etc.) and hubs can be connected to the USB Host in the USB tiered-star topology.

The specification for standard USB states that each USB port be capable of providing 5 volts at 500 ma. This provision is strictly dependent on the power supply used with the iPac. Obviously the power supply must be able to source 5 volts at 1 amp for the USB requirement in addition to the other power requirements of the board. A single 1100 mA automatic reset Polyfuse is used to protect the USB outputs from shorts. There is no provision to turn off power to the USB ports.

2.15 SOK1: MMC/SD Flash Card Socket

The iPac 9302 provides standard 5638 type socket, which accepts SD, MMC, and SDIO cards. This Socket is connected to the processor's SPI bus and uses the SPI mode provided by both SD and MMC standards. Pins 8-11 provide the expanded optional connections added by the Secure Digital standard, they are connected to the CPLD for flexibility. A red LED (LD1) indicates when the Flash card is being accessed. The card can be hot-swapped although care should be taken not to remove the card while its being accessed.

Table 8: MMC/SD SOCKET (SOK1)

Pin	Signal	Description
1	EGPIO_[8]/MMCSD_~SEL	Card Select
2	SSPTX1	SI
3	GND	GND
4	3.3 Volts	VCC
5	SCK1	SCK
6	GND	GND
7	SSPRX1	SO
8	PLD	IRQ
9	NC	-
10	PLD	CD
11	PLD	WPGND
12	GND	EXGND

2.16 Real-Time Clock

The iPac 9302 is equipped on some models with an external, battery-backed, Real-Time Clock (RTC). The EP9302 processor provides an internal RTC but there is no provision for battery backing it. The external RTC is based on the I2C ISL1208 chip from Intersil. The EP9302 does not have a true I2C interface but does offer a couple of lines that can act in that capacity. These are referred to as EECLK and EEDAT. Since there is no I2C circuitry, bit-banging these two lines is required.

In addition, processor line FGPIO[3]/RTC_~INTRQ is connected to the IRQ line of the RTC. Using this line the RTC can wake the processor up from sleep modes on the second, minute, hour, day of the week, or month. The RTC also offers 2 bytes of battery-backed RAM and 15 selectable frequency outputs.

2.17 EEPROM

Also equipped on some models is 256K Bytes of SPI based EEPROM. To select this device SFRM1 (SPI Frame) and EGPIO[7]/EE_SEL are logically ORed together. The SFRM1 signal is automatically generated so control comes from the EGPIO[7]/EE_SEL line. SO, SI, SCLK of the EEPROM are connected to SSPRX1, SSPTX1, and SSCLK1 respectively. The EEPROM is handy place to store the MAC address and other configuration data.

3. Software

3.1 Introduction

The iPac 9302 can be programmed in a variety of languages and utilize a variety of Operating Systems. There are a number of Free compilers, interpreters, and assemblers available allowing the iPac to be programmed in C, BASIC or Assembly languages. EMAC has Board Support Packages available for Linux, Windows CE, and .NET Micro Framework. For more information on these particular Operating Systems, contact EMAC, Inc.

3.2 Loading Your Software

The resident flash on the iPac can be programmed via the JTAG or by the following methods:

3.2.1 DOWNLOAD.EXE

Cirrus Logic provides a PC based utility, download.exe, which allows you to download code to on-board flash via UART1. Instructions for use and the actual application source code are available on the Cirrus website. This requires the proper configuration of JB4.

3.2.2 EBOOT.NB0

This is a bootloader that is included with the Windows CE BSP. If it is loaded in the on-board flash, it allows you to quickly download CE builds to the iPac's RAM or flash via Ethernet. This bootloader can be loaded to the board using the download.exe utility.

3.2.3 RedBoot™

Cirrus Logic provides a port of the eCos-2.0 RedBoot bootloader [9] for the EP9302. This bootloader, included with the Linux support option, is capable of booting both Linux and Windows CE, and can execute independently of user intervention through a scripted flash interface. . This bootloader can be loaded to the board using the download.exe utility.

RedBoot™ is an acronym for "Red Hat Embedded Debug and Bootstrap", and is the standard embedded system debug/bootstrap environment from Red Hat, replacing the previous generation of debug firmware: CygMon and GDB stubs. It provides a complete bootstrap environment for a range of embedded operating systems, such as embedded Linux™ and eCos™, and includes facilities such as network downloading and debugging. It also provides a simple flash file system for boot images.

RedBoot provides a wide set of tools for downloading and executing programs on embedded target systems, as well as tools for manipulating the target system's environment. It can be used for both product development (debug support) and for end product deployment (flash and network booting).

Here are some highlights of RedBoot's capabilities:

- Boot scripting support
- Simple command line interface for RedBoot configuration and management, accessible via serial (terminal) or Ethernet (telnet)
- Integrated GDB stubs for connection to a host-based debugger via serial or ethernet. (Ethernet connectivity is limited to local network only)
- Attribute Configuration - user control of aspects such as system time and date (if applicable), default Flash image to boot from, default failsafe image, static IP address, etc.
- Configurable and extensible, specifically adapted to the target environment
- Network bootstrap support including setup and download, via BOOTP, DHCP and TFTP
- X/YModem support for image download via serial
- Power On Self Test

Although RedBoot is derived from eCos, it may be used as a generalized system debug and bootstrap control software for any embedded system and any operating system. For example, with appropriate additions, RedBoot could replace the commonly used BIOS of PC (and certain other) architectures. Red Hat is currently installing RedBoot on all embedded platforms as a standard practice, and RedBoot is now generally included as part of all Red Hat Embedded Linux and eCos ports. Users who specifically wish to use RedBoot with the eCos operating system should refer to the Getting Started with eCos document, which provides information about the portability and extendibility of RedBoot in an eCos environment.

The existing Cirrus build environment provides a single directory in which the bootloader, OS, and windowing environment are created from a single build script. To speed development time, code specific to the RedBoot environment was extracted into a separate standalone project.

4. PCD-39E00 Terminal Board

4.1 Introduction

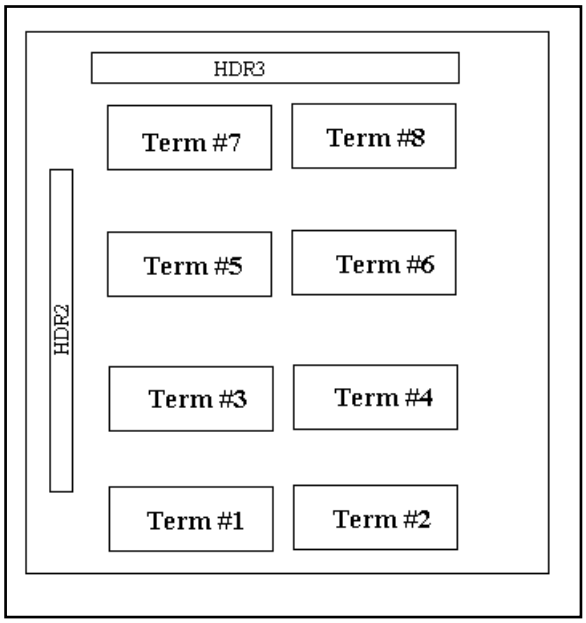
The PCD-39E00 is a Terminal Board that can be used with the iPac series of SBCs as well as other products. This Terminal Board is designed to be used stacked on top of the iPac using the supplied standoffs but can be alternatively used off to the side if the user provides longer cables.

The PCD-39E00 comes with three cables of which only two can be used at one time. The HRD2 (Analog) connector is always used if Analog connectivity is required whereas HDR1 and HDR3 are selectively used depending on the desired connectivity. If HDR3 has the desired connectivity then use the short 50 pin ribbon cable. If HDR1 connectivity is desired then the long twisted cable should be used. Note the twist needs to be intact.

If connectivity to both HDR3 and HDR1 are necessary then two PCD-39E00s will be required, one which uses the short 50 pin cable and the other that uses the longer 50 pin cable with the twist.

4.2 iPac Terminal Board Pin-Out

The PCD-39E00 can be used with several different boards thereby changing the connector descriptions for each board. Therefore the specific iPac descriptions are given within the context of the iPac manual. There are eight individual 10-pin screw terminal connectors used on the PCD-39E00. Each is labeled STx where x is numbered from 1 to 8. The diagram below shows the connector layout.



The connection of the PCD-39E00 when connected to an iPac HDR2 and HDR3 are as follows:

Screw Terminal	IPAC HDR3	Description	Screw Terminal	IPAC HDR2	Description
Term 5, Pin 1	Gnd	Gnd	Term 1, Pin 1	HDR2, Pin 39	5V
Term 5, Pin 2	HDR3, Pin 1	Port 2.7 (PH3)	Term 1, Pin 2	HDR2, Pin 1	A/D0
Term 5, Pin 3	HDR3, Pin 3	Port 2.6 (PH2)	Term 1, Pin 3	HDR2, Pin 2	A/D1
Term 5, Pin 4	Gnd	Gnd	Term 1, Pin 4	HDR2, Pin 3	A/D2
Term 5, Pin 5	HDR3, Pin 5	Port 2.5 (PP5)	Term 1, Pin 5	HDR2, Pin 4	A/D3
Term 5, Pin 6	HDR3, Pin 7	Port 2.4 (PP4)	Term 1, Pin 6	HDR2, Pin 5	A/D4
Term 5, Pin 7	Gnd	Gnd	Term 1, Pin 7	HDR2, Pin 6	A/D5
Term 5, Pin 8	HDR3, Pin 9	Port 2.3 (PP3)	Term 1, Pin 8	HDR2, Pin 7	A/D6
Term 5, Pin 9	HDR3, Pin 11	Port 2.2 (PP2)	Term 1, Pin 9	HDR2, Pin 8	A/D7
Term 5, Pin 10	Gnd	Gnd	Term 1, Pin 10	Gnd	Gnd
Term 6, Pin 1	HDR3, Pin 13	Port 2.1 (PP1)	Term 2, Pin 11	HDR2, Pin 39	5V
Term 6, Pin 2	HDR3, Pin 15	Port 2.0 (PP0)	Term 2, Pin 12	HDR2, Pin 9	A/D8
Term 6, Pin 3	Gnd	Gnd	Term 2, Pin 13	HDR2, Pin 10	A/D9
Term 6, Pin 4	HDR3, Pin 17	Port 1.7 (PT7)	Term 2, Pin 14	HDR2, Pin 11	A/D10
Term 6, Pin 5	HDR3, Pin 19	Port 1.6 (PT6)	Term 2, Pin 15	HDR2, Pin 12	A/D11
Term 6, Pin 6	Gnd	Gnd	Term 2, Pin 16	HDR2, Pin 13	A/D12
Term 6, Pin 7	HDR3, Pin 21	Port 1.5 (PT5)	Term 2, Pin 17	HDR2, Pin 14	A/D13
Term 6, Pin 8	HDR3, Pin 23	Port 1.4 (PT4)	Term 2, Pin 18	HDR2, Pin 15	A/D14
Term 6, Pin 9	Gnd	Gnd	Term 2, Pin 19	HDR2, Pin 16	A/D15
Term 6, Pin 10	HDR3, Pin 49 (5V)	5V	Term 2, Pin 20	Gnd	Gnd
Term 7, Pin 1	Gnd	Gnd	Term 3, Pin 1	HDR2, Pin 39	5V
Term 7, Pin 2	HDR3, Pin 25	Port 1.3 (PT3)	Term 3, Pin 2	HDR2, Pin 40	+Vin
Term 7, Pin 3	HDR3, Pin 27	Port 1.2 (PT2)	Term 3, Pin 3	HDR2, Pin 19	D/A0
Term 7, Pin 4	Gnd	Gnd	Term 3, Pin 4	HDR2, Pin 20	D/A1
Term 7, Pin 5	HDR3, Pin 29	Port 1.1 (PT1)	Term 3, Pin 5	Gnd	Gnd
Term 7, Pin 6	HDR3, Pin 31	Port 1.0 (PT0)	Term 3, Pin 6	HDR2, Pin 23	D/A2
Term 7, Pin 7	Gnd	Gnd	Term 3, Pin 7	HDR2, Pin 24	D/A3
Term 7, Pin 8	HDR3, Pin 33	Port 0.7 (PA7)	Term 3, Pin 8	HDR2, Pin 25	D/A4
Term 7, Pin 9	HDR3, Pin 35	Port 0.6 (PA6)	Term 3, Pin 9	HDR2, Pin 26	D/A5
Term 7, Pin 10	Gnd	Gnd	Term 3, Pin 10	Gnd	Gnd
Term 8, Pin 1	HDR3, Pin 37	Port 0.5 (PA5)	Term 4, Pin 11	HDR2, Pin 39	5V
Term 8, Pin 2	HDR3, Pin 39	Port 0.4 (PA4)	Term 4, Pin 12	HDR2, Pin 29	A/D16
Term 8, Pin 3	Gnd	Gnd	Term 4, Pin 13	HDR2, Pin 30	A/D17
Term 8, Pin 4	HDR3, Pin 41	Port 0.3 (PA3)	Term 4, Pin 14	HDR2, Pin 31	A/D18
Term 8, Pin 5	HDR3, Pin 43	Port 0.2 (PA2)	Term 4, Pin 15	HDR2, Pin 32	A/D19
Term 8, Pin 6	Gnd	Gnd	Term 4, Pin 16	HDR2, Pin 33	A/D20
Term 8, Pin 7	HDR3, Pin 45	Port 0.1 (PA1)	Term 4, Pin 17	HDR2, Pin 34	A/D21
Term 8, Pin 8	HDR3, Pin 47	Port 0.0 (PA0)	Term 4, Pin 18	HDR2, Pin 35	A/D22
Term 8, Pin 9	Gnd	Gnd	Term 4, Pin 19	HDR2, Pin 36	A/D23
Term 8, Pin 10	HDR3, Pin 49 (5V)	5V	Term 4, Pin 20	Gnd	Gnd

The connection of the PCD-39E00 when connected to an iPac HDR1 and HDR2 are as follows:

Screw Terminal	IPAC HDR1	Description	Screw Terminal	IPAC HDR2	Description
Term 5, Pin 1	Gnd	Gnd	Term 1, Pin 1	HDR2, Pin 39	5V
Term 5, Pin 2	HDR1, Pin 1	Port 2.7 (Y7)	Term 1, Pin 2	HDR2, Pin 1	A/D0
Term 5, Pin 3	HDR1, Pin 3	Port 2.6 (Y6)	Term 1, Pin 3	HDR2, Pin 2	A/D1
Term 5, Pin 4	Gnd	Gnd	Term 1, Pin 4	HDR2, Pin 3	A/D2
Term 5, Pin 5	HDR1, Pin 5	Port 2.5 (Y5)	Term 1, Pin 5	HDR2, Pin 4	A/D3
Term 5, Pin 6	HDR1, Pin 7	Port 2.4 (Y4)	Term 1, Pin 6	HDR2, Pin 5	A/D4
Term 5, Pin 7	Gnd	Gnd	Term 1, Pin 7	HDR2, Pin 6	A/D5
Term 5, Pin 8	HDR1, Pin 9	Port 2.3 (Y3)	Term 1, Pin 8	HDR2, Pin 7	A/D6
Term 5, Pin 9	HDR1, Pin 11	Port 2.2 (Y2)	Term 1, Pin 9	HDR2, Pin 8	A/D7
Term 5, Pin 10	Gnd	Gnd	Term 1, Pin 10	Gnd	Gnd
Term 6, Pin 1	HDR1, Pin 11	Port 2.1 (Y1)	Term 2, Pin 11	HDR2, Pin 39	5V
Term 6, Pin 2	HDR1, Pin 15	Port 2.0 (Y0)	Term 2, Pin 12	HDR2, Pin 9	A/D8
Term 6, Pin 3	Gnd	Gnd	Term 2, Pin 13	HDR2, Pin 10	A/D9
Term 6, Pin 4	HDR1, Pin 17	Port 1.7 (X7)	Term 2, Pin 14	HDR2, Pin 11	A/D10
Term 6, Pin 5	HDR1, Pin 19	Port 1.6 (X6)	Term 2, Pin 15	HDR2, Pin 12	A/D11
Term 6, Pin 6	Gnd	Gnd	Term 2, Pin 16	HDR2, Pin 13	A/D12
Term 6, Pin 7	HDR1, Pin 21	Port 1.5 (X5)	Term 2, Pin 17	HDR2, Pin 14	A/D13
Term 6, Pin 8	HDR1, Pin 23	Port 1.4 (X4)	Term 2, Pin 18	HDR2, Pin 15	A/D14
Term 6, Pin 9	Gnd	Gnd	Term 2, Pin 19	HDR2, Pin 16	A/D15
Term 6, Pin 10	HDR1, Pin 49 (5V)	5V	Term 2, Pin 20	Gnd	Gnd
Term 7, Pin 1	Gnd	Gnd	Term 3, Pin 1	HDR2, Pin 39	5V
Term 7, Pin 2	HDR1, Pin 25	Port 1.3 (X3)	Term 3, Pin 2	HDR2, Pin 40	+Vin
Term 7, Pin 3	HDR1, Pin 27	Port 1.2 (X2)	Term 3, Pin 3	HDR2, Pin 19	D/A0
Term 7, Pin 4	Gnd	Gnd	Term 3, Pin 4	HDR2, Pin 20	D/A1
Term 7, Pin 5	HDR1, Pin 29	Port 1.1 (X1)	Term 3, Pin 5	Gnd	Gnd
Term 7, Pin 6	HDR1, Pin 31	Port 1.0 (X0)	Term 3, Pin 6	HDR2, Pin 23	D/A2
Term 7, Pin 7	Gnd	Gnd	Term 3, Pin 7	HDR2, Pin 24	D/A3
Term 7, Pin 8	HDR1, Pin 33	Port 0.7 (Z2)	Term 3, Pin 8	HDR2, Pin 25	D/A4
Term 7, Pin 9	HDR1, Pin 35	Port 0.6 (Z1)	Term 3, Pin 9	HDR2, Pin 26	D/A5
Term 7, Pin 10	Gnd	Gnd	Term 3, Pin 10	Gnd	Gnd
Term 8, Pin 1	HDR1, Pin 37	Port 0.5 (Z0)	Term 4, Pin 11	HDR2, Pin 39	5V
Term 8, Pin 2	HDR1, Pin 39	Port 0.4 (E4)	Term 4, Pin 12	HDR2, Pin 29	A/D16
Term 8, Pin 3	Gnd	Gnd	Term 4, Pin 13	HDR2, Pin 30	A/D17
Term 8, Pin 4	HDR1, Pin 41	Port 0.3 (E3)	Term 4, Pin 14	HDR2, Pin 31	A/D18
Term 8, Pin 5	HDR1, Pin 43	Port 0.2 (E2)	Term 4, Pin 15	HDR2, Pin 32	A/D19
Term 8, Pin 6	Gnd	Gnd	Term 4, Pin 16	HDR2, Pin 33	A/D20
Term 8, Pin 7	HDR1, Pin 45	Port 0.1 (E1)	Term 4, Pin 17	HDR2, Pin 34	A/D21
Term 8, Pin 8	HDR1, Pin 47	Port 0.0 (E0)	Term 4, Pin 18	HDR2, Pin 35	A/D22
Term 8, Pin 9	Gnd	Gnd	Term 4, Pin 19	HDR2, Pin 36	A/D23
Term 8, Pin 10	HDR1, Pin 49 (5V)	5V	Term 4, Pin 20	Gnd	Gnd

