MitiPy™

User Manual

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(for use with Rev 1 Boards)

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1 Introduction

This document describes EMAC's MitiPy Industrial IoT device. The MitiPy is an Industrial IoT device that is designed to provide a secure, flexible and ruggedized Industrial IOT Gateway solution. The MitiPy is built around the STMicroelectronics STM32 microcontroller, which provides several of its key features. The MitiPy provides a comprehensive wireless multi-protocol (Wi-Fi + BT5) connectivity solution. Additionally, the MitiPy supports both the Skywire Cellular Module(s) and the MultiConnect mDot LoRa module. This module also provides RS232, RS485, CAN, USB and Ethernet to support protocols such as Modbus, PROFINET and EtherCAT.

In addition to the features listed below, the MitiPy also features a fast 32-bit core, open source software support, and a wide range of controller I/O pins.

1.1 Features

- **STMicroelectronics ARM Cortex-M4 168MHz**
- **Up to 1M of Flash**
- **192 Kbytes of SRAM**
- **10Base-T / 100Base-TX Ethernet (optional)**
- **POE 802.3af (optional)**
- **1x microSD Card Slot**
- **1x CAN 2.0B Port (Internal provided w/Transceiver, External provided w/o Transceiver)**
- **2x USB 2.0 Ports (1x Internal Full Speed OTG w/ PHY, 1x External Full-Speed Device)**
- **4x Serial Ports**
  - 1x RS232 & 1x RS232/422/485 (Internal)
  - 2x TTL (External)
- **1x SPI Port**
- **2x I2C Hardware Ports**
- **25x Timer/Counters/PWM/Capture**
- **RTC with on-board battery backup**
- **Internal Temperature Sensor**
- **1x Reset Button**
- **13x A/D Channels with 12-bit Resolution (3 Unique A/Ds)**
- **2x D/A Channels with 12-bit Resolution**
- **18x External Dedicated GPIOs (64x fully allocated)**
- **8x High-Drive Open Collector Outputs (w/ LEDs)**
- **2x 50-Pin Expansion Headers**
- **1x User Button**
- **2x User LEDs**

- **OS/Language: MicroPython or FreeRTOS**
- **Redpine RS9113/RS9116 (Wi-Fi + BT5) (optional)**
  - **802.11 b/g/n/j Wi-Fi**
  - **802.15.1 Bluetooth (BT 5.0)**
- **Skywire Cellular Module (optional)**
  - **4G LTE CAT M1, CAT NB1, CAT 1, CAT 3, CAT 4**
  - **3G HSPA+**
  - **2G GSM (Fallback)**
  - **XBee Socket**
- **MultiConnect mDot LoRa Module (optional)**
  - **LoRaWAN**
  - **XBee Socket**

1.2 MitiPy Specifications

- **CPU:** STM32F407IGH6 ARM Cortex-M4 w/Math Coprocessor
- **Flash:** Up to 1MB of Flash
- **RAM:** 192 KB of SRAM
- **Ethernet:** 10Base-T / 100Base-TX
- **POE:** 802.3af
- **Flash Disk:** Micro SD Card Socket
- **System Reset:** Supervisor with external Reset Button provision
- **RTC:** Battery backed Real Time Clock
- **Timer/Counters:** 25x Timer/Counter/PWM/Capture
- **Digital I/O:** 18x External Dedicated GPIOs (64x fully allocated)
- **Analog I/O:**
  - 13x A/D Channels with 12-bit Resolution (3 Unique A/Ds)
  - 2x D/A Channels with 12-bit Resolution
- **Power:**
  - Wide-Input Locking Terminal Block Header
  - POE (802.3af)
- **JTAG:** Processor JTAG Supporting Programming, Trace, and Boundary Scan

1.3 Serial Interfaces

- **UARTS:** 1x RS232, 1x RS232/422/485, 2x TTL
- **SPI:** 1x SPI Ports
- **USB:** 2x USB 2.0 Ports
  - 1x Full-Speed OTG terminating to a micro USB connector (Internal)
  - 1x Full-Speed Device terminating to a header connector (External)
- **I2C:** 2x I2C hardware Ports

1.4 Mechanical and Environmental

- **Dimensions:** 6.05" × 4.38"
- **Power Supply Voltage:** 8VDC ~ 36VDC or POE
- **Power Requirements (typical):**
  - 12.0 Volts @ 40.00mA (0.480 watts)
  - Max current draw during boot process: TBD
  - Constant busy loop: TBD
  - Idle system: TBD
  - Idle system with Ethernet PHY disabled: TBD
  - APM sleep mode with Ethernet PHY disabled: TBD
  - APM sleep mode with Ethernet PHY enabled: TBD
- **Operating Temperature:** -40 ~ 85° C (-40 ~ 185 ° F)
- **Operating Humidity:** 0% ~ 90% relative humidity, non-condensing

2 MitiPy Product Details

2.1 Jumper Configuration & Connector Descriptions

The MitiPy comes factory configured. In the event that jumpers need to be verified or modified, this section provides the information required including instructions on setting jumpers and connecting peripherals, switches, and indicators. Be sure to read all the safety precautions before you begin any configuration procedure. See Appendix A for connector pinouts and Appendix B for Jumper Setting descriptions.

Table 1: Jumpers

Label	Function	Default
JB1	Boot0 Source Selection	FLS
JB2	Boot1 Source Selection	ROM
JB3	RTC & RAM Retention Battery	OFF
JB4	CAN Termination	OFF
JB5	SOK2 Power Supply Voltage Option	3V3
JB6	SOK3 Power Supply Voltage Option	3V3

Table 2: Connectors

Label	Function
CN1	Serial Port COM A
HDR1	I/O Header
HDR2	I/O Header
HDR3	MCU JTAG/SWD
HDR4	HS CAN 2.0B Port
HDR5	Serial Port COM B
JK1	USB OTG
JK2	Ethernet RJ45
SOK1	MicroSD Socket
SOK2	Skywire Cellular Module Socket
SOK3	MultiConnect mDot LoRa Module Socket
ST1	Power Supply Terminal Block

2.2 Power Connectors

The MitiPy provides one main wide-input locking DC power supply connector (ST1). ST1 is a Phoenix Contact 3-pin terminal block header (Part # 1817628) and mates with Phoenix Contact 3-pin terminal block plug (Part # 1817246). ST1 includes a Chassis Ground connection for increased signal integrity and system stability.

Optionally, the MitiPy can be powered through POE (802.3af) on RJ45 jack (JK2). See Power over Ethernet section below for additional details.

The Input voltage (Vin) 8VDC ~ 36VDC or 12VDC (POE) can be used to pull-up HiDrive Outputs by connecting HDR1 pin-5 and pin-6 together.

Table 3: Power Supply Terminal Block (ST1)

Pin	Signal
1	Vin
2	GND
3	Chassis GND

2.3 Ethernet (optional)

The MitiPy provides a 10Base-T / 100Base-TX Ethernet port with auto MDI/MDI-X for reliable detection of and correction for straight-through and crossover cables. The ethernet interface is accessible on RJ45 (JK2) which includes integrated link and activity LEDs.

2.4 Power over Ethernet (optional)

The MitiPy supports Power over Ethernet (POE) 802.3af. The POE capability increases the systems flexibility and ability to be deployed into environments where external power supplies may not be available or feasible. Note: The POE interface will provide 12VDC to HDR1 pin-5 which can be used as the HiDrive Output(s) interface voltage by connecting HDR1 pin-5 and pin-6.

2.5 Serial Ports

The MitiPy is equipped with four serial ports. One RS-232 serial port terminating to a male DB9 connector (COM A), one RS-232/422/485 multi-mode serial port terminating to a 10-pin header (COM B), and two TTL USARTs accessed through I/O header 2 (HDR2).

- The RS-232 serial port (COM A) terminates to male DB9 connector at CN1. The RS-232 Transceiver (U6) limits the maximum throughput to 250 kb/s. The transceiver can be placed in standby mode by holding GPIO PE1 low. In standby mode the transceiver will typically draw 1µA. When the device is powered down the receivers remain active and the drivers are placed in a high-impedance state.

- RS-232/422/485 (software-configurable) serial port (COM B) terminates to 10-pin header located at HDR5. By default, the RS-232 transceiver (U10) and the RS-422/485 transceiver (U9) are in standby mode. In standby mode, the RS-232 transceiver typically draws 1µA and the RS-422/485 transceiver typically draws 0.1µA. Both devices' driver and receiver output(s) will be high-impedance while in standby mode. To configure RS-232 mode, GPIO PE2 should be held high. The maximum throughput for RS-232 is 250 Kb/s. To configure RS-422/485 mode, GPIO PF11 should be held high and the maximum throughput in this mode is 2.62Mb/s (Oversampling by 16) and 5.25 Mb/s (Oversampling by 8). Note: The RS422/485 transceiver includes a logic selectable 120Ω termination resistor. To enable the termination resistor GPIO PF0 should be held high.

- The TTL serial ports (USARTs 1 & 6) are accessible on I/O header HDR2. USART1 provides for bidirectional communication offering Tx and Rx lines with a maximum bit rate of 10.5 Mb/s. USART6 provides for bidirectional communication offering Tx, Rx, CTS, RTS, and CK lines with Synchronous Mode and Hardware Flow Control Mode. The maximum bit rate for this is 10.5Mb/s. The USARTs also support LIN, Smartcard Protocol, and IrDA.

Table 4: Serial Port - COM A (CN1)

Pin	DB9 Connector: Description
1	NC
2	RXD
3	TXD
4	NC
5	GND
6	NC
7	RTS
8	CTS
9	NC

Table 5: Serial Port - COM B (HDR5)

Pin	10-Pin Header: Description (RS-232)	10-Pin Header Description (RS-485/422)
1	NC	TX-
2	NC	NC
3	RXD	TX+
4	RTS	NC
5	TXD	RX+
6	CTS	NC
7	NC	RX-
8	NC	NC
9	GND	GND
10	NC	NC

Table 6: Serial Port - USART1 & USART6 (HDR2)

Pin	Utility I/O 2 Pinout
38	USART1_TXD_3V
39	USART1_RXD_3V
40	USART6_CLK_3V
41	USART6_TXD_3V
42	USART6_RXD_3V
43	USART6_CTS_3V
44	USART6_RTS_3V

2.6 USB Ports

The MitiPy provides one USB 2.0 Full-Speed (FS) On-The-Go (OTG) port and one USB 2.0 High-Speed (HS) / Full-speed (FS) On-The-Go (OTG) interface. The USB OTG port is accessible on the micro USB connector (JK1). Note: The external power switch (U12) must be enabled to supply power to a connected device in host mode applications. To enable the USB power switch GPIO PA8 must be held high.

The USB HS/FS OTG interface is accessible on I/O header HDR1. Use of the USB interface in combination with the USB FS OTG port (JK1) requires an external FS/HS transceiver solution. The interface's OTG implementation requires an external USB VBUS switch solution.

Both USB Ports support the Sessions Request Protocol (SRP) and soft disconnect features.

The Table below calls out the necessary connections for the USB HS/FS OTG Interface.

Table 7: USB HS Interface Pin Assignments (HDR1 & HDR2)

Pin	MitiPy Pin Name	USB ULPI Pin Name
HDR2: 34 or 15	PI11 or ADC123_IN12 (PC2)	OTG_HS_ULPI_DIR
HDR2: 16 or 24	ADC123_IN13 (PC3) or I2C2_SCL (PH4)	OTG_HS_ULPI_NXT
HDR2: 14	ADC123_IN10 (PC0)	OTG_HS_ULPI_STP
HDR2: 21	DAC_OUT2 (PA5)	OTG_HS_ULPI_CK
HDR2: 7	ADC123_IN3 (PA3)	OTG_HS_ULPI_D0
HDR2: 18	ADC12_IN8 (PB0)	OTG_HS_ULPI_D1
HDR2: 19	ADC12_IN9 (PB1)	OTG_HS_ULPI_D2
HDR1: 16	TIM2_CH3 (PB10)	OTG_HS_ULPI_D3
HDR1: 17	TIM2_CH4 (PB11)	OTG_HS_ULPI_D4
HDR2: 32	SPI-1_MOSI (PB5)	OTG_HS_ULPI_D7
HDR1: 45	USB_OTG_HS_ID (PB12)	*OTG_HS_ID / OTG_HS_ULPI_D5
HDR1: 46	USB_OTG_HS_VBUS (PB13)	*OTG_HS_VBUS / OTG_HS_ULPI_D6
HDR1: 47	USB_OTG_HS_D_N (PB14)	*OTG_HS_DM
HDR1: 48	USB_OTG_HS_D_P (PB15)	*OTG_HS_DP

* indicates Full-Speed lines

2.7 MicroSD Card Socket

The MitiPy provides a high capacity MicroSD socket (SOK1). This socket is hot-swappable and can accept a wide variety of Flash Cards. A card that is written to by the MitiPy can be read by another computer using a MicroSD card reader. The MicroSD interface is compatible with Standard and High Capacity MicroSD cards.

2.8 CAN Port

The MitiPy provides a High-Speed CAN 2.0B port utilizing the TI TCAN332GDCNT Transceiver (U5). The CAN port is accessible on the 3-pin header (HDR4). HDR4 is a TE Connectivity 3-pin locking header (Part # 640456-3) and mates with TE Connectivity 3-pin housing (Part # 1375820-3). Note: The MitiPy includes a jumper-selectable 120Ω CAN bus termination resistor. To enable the termination resistor place jumper JB4 in the TRM position.

Table 8: CAN (HDR4)

Pin	Signal
1	CAN_H
2	CAN_L
3	GND

2.9 Real-Time Clock

The MitiPy is equipped with an external battery (B1) for backing up the Real-Time Clock (RTC). Drivers to access the RTC are included in the operating systems. Jumper JB3 should be placed in the ON position in order to retain system time when powered down.

2.10 Temperature Sensor

The MitiPy is equipped with an internal temperature sensor located in the STM32 microcontroller that can be used to measure the ambient temperature of the device. ADC1_IN16 channel is used to convert the sensor output voltage to a digital value.

2.11 Reset

The MitiPy is equipped with a reset push-button (PB1). Pressing this button will execute a hardware reset of the system.

2.12 User Button and LEDs

The MitiPy is equipped with a user push-button (PB2) and two user programmable LEDs (LD11). The push-button provides the user with an additional input and can be used to reset the MicroPython filesystem to default.

2.13 Wireless (optional)

The MitiPy features the RedPine RS9116 Wireless Radio Module which provides a comprehensive multi-protocol wireless connectivity solution including 802.11 b/g/n (2.4GHz), 802.11j and dual-mode Bluetooth 5.0. The module provides a U.FL connector for the primary external antenna connection. EMAC can provide a compatible antenna kit upon request.

The RS9116 module is highly configurable supporting numerous radio operating modes and multiple power modes to reduce the module's power consumption. Some of the features include:

Wi-Fi:

- Compliant to single-spatial stream IEEE 802.11 b/g/n, 802.11j with single or dual band support
- Support for 20 MHz and 40 MHz channel bandwidths
- Operating Frequency Range: 2412 MHz - 2484 MHz
- Transmit power up to +20dBm with integrated PA
- Receive sensitivity as low as -97 dBm

Bluetooth:

- Compliant to dual-mode Bluetooth 5
- Operating Frequency Range: 2.402 GHz - 2.480 GHz
- Receive sensitivity as low as -104 dBm

RF Features:

- Integrated baseband processor with calibration memory, RF transceiver, high-power amplifier, balun and T/R switch
- Integrated Antenna and u.FL connector

The MCU can issue an ultra-low power (ULP) wakeup to the module by pulling GPIO PB9 high.

The module provides both a host wakeup signal, GPIO PG12 (active-high), and a module ULP sleep indicator, GPIO PE5 (active-low). A module reset can be issued by pulling GPIO PE3 low.

2.14 Socket Modules (optional)

The MitiPy provides for two module sockets, SOK2 and SOK3, that are compatible with the XBee/XBee-PRO module form factor and pinout.

Socket (SOK2) is specifically designed to support NimbeLink's Skywire Cellular Module(s). The Skywire family of end-device certified cellular modules are pin compatible and support numerous cellular technologies. The modules provide a U.FL connector for the primary cellular antenna connection and Micro SIM card socket for network flexibility. Depending on the primary cellular technology the Skywire cellular modules include 2G/3G fallback and integrated GPS/GNSS radios features with dedicated U.FL antenna connectors. EMAC can provide a compatible antenna kit upon request.

Some Skywire modems feature an on-board soldered-down chip SIM that can be used in place of a removable Micro SIM card. This chip SIM is specific to one carrier. By default, the modem is configured to attempt to use the external SIM card. However, users can select which SIM the modem is using by controlling the on-board SIM selection switch with AT commands.

The Skywire modules have FOTA (Firmware over the Air) capability. However, USB connector JK3 can be populated to facilitate on-board firmware updates and debugging if necessary.

The MitiPy provides two slot holes to be used in conjunction with a zip-tie to achieve maximum module retention for rigorous industrial environments. Systems utilizing an enclosure can use other mechanical retention methods if desired.

The MitiPy also provides a jumper-selectable voltage supply feature which allows the system to supply either 3.3VDC or 3.8VDC to the socket module. Jumper (JB5) should be installed in 3V8 position when utilizing Skywire Cellular Modules. By default, the module is off. GPIO PD10 must be held high to turn on the module.

The MitiPy provides a module status LED (LD12) to provide the user a visual indicator of the module's operation status. In addition, GPIO PF1 will be pulled low when the module is on. A module reset can be issued by pulling GPIO PE3 low.

Socket (SOK3) is specifically designed to support MultiTech's MultiConnect mDot LoRa Module.

The MultiConnect mDot is a programmable, end-device certified, long-range RF module that provides encrypted data connectivity to sensors, industrial equipment and remote appliances. By using LoRa Long Range Spread Spectrum technology, bidirectional data communication can be maintained for distances up to 5 miles line of sight, deep into buildings, or within noisy environments using unlicensed ISM bands. Actual distance depends on conditions, configurations, antennas, desired throughput and usage frequency. In dense urban environments, a typical range is 1-2 miles. The module provides a U.FL connector for the primary external antenna connection. EMAC can provide a compatible antenna kit upon request.

The MultiConnect mDot modules have FOTA (Firmware over the Air) capability. However, cortex-m debug header HDR9 and module header(s) HDR8 can be populated to facilitate on-board firmware updates and debugging if necessary.

The MitiPy provides one standoff (STO1) to be used in conjunction with a M2.5 X 5mm pan-head screw to achieve maximum module retention for rigorous industrial environments.

The MitiPy also provides a jumper-selectable voltage supply feature which allows the system to supply either 3.3VDC or 5.0VDC to the socket module. Jumper (JB6) should be installed in 5V0 position when utilizing MultiConnect mDot Modules. A module reset can be issued by pulling GPIO PE3 low.

2.15 I/O Expansion

The MitiPy provides access to a number of I/O lines on connectors HDR1 and HDR2. The 50-pin dual row headers contain GPIO lines, USB, UART, SPI bus, I²C bus, CAN bus, A/D lines, interrupts, high drive outputs, and power pins. The tables below list the pinouts and the corresponding signals for both I/O headers.

Table 9: I/O Header (HDR1)

Pin#	Signal	MCU Pin Name	MCU Pin Number	Pin#	Signal	MCU Pin Name	MCU Pin Number
1	GND	N/A	N/A	**2**	GND	N/A	N/A
3	3V3_VCC	N/A	N/A	**4**	5V0_VCC	N/A	N/A
5	VIN	N/A	N/A	**6**	V_HIDRV	N/A	N/A
7	TIM1_ETR	PE7	R8	**8**	TIM1_CH1N	PE8	P8
9	TIM1_CH1	PE9	P9	**10**	TIM1_CH2N	PE10	R9
11	TIM1_CH2	PE11	P10	**12**	TIM1_CH3N	PE12	R10
13	TIM1_CH3	PE13	N11	**14**	TIM1_CH4	PE14	P11
15	TIM1_BKIN	PE15	R11	**16**	TIM2_CH3	PB10	R12
17	TIM2_CH4	PB11	R13	**18**	TIM3_CH2	PC7	G15
19	TIM4_CH2	PD13	M15	**20**	TIM4_ETR	PE0	A4
21	TIM4_CH3	PD14	M14	**22**	GND	N/A	N/A
23	TIM5_CH1	PH10	L13	**24**	TIM4_CH4	PD15	L14
25	TIM5_CH3	PH12	K12	**26**	TIM5_CH2	PH11	L12
27	TIM8_CH3N	PH15	D13	**28**	TIM8_CH2N	PH14	E13
29	TIM8_CH1	PI5	C4	**30**	TIM8_BKIN	PI4	D4
31	TIM8_CH3	PI7	C2	**32**	TIM8_CH2	PI6	C3
33*	HD_PG1	PG1	M7	**34***	HD_PG0	PG0	N7
35*	HD_PG3	PG3	K15	**36***	HD_PG2	PG2	L15
37*	HD_PG5	PG5	K13	**38***	HD_PG4	PG4	K14
39*	HD_PG10	PG10	B10	**40***	HD_PG6	PG6	J15
41	PF12	PF12	P6	**42**	PF13	PF13	N6
43	PF14	PF14	R7	**44**	PF15	PF15	P7
45	OTG_HS_ID	PB12	P12	**46**	OTG_HS_VB	PB13	P13
47	OTG_HS_DM	PA11	R14	**48**	OTG_HS_DP	PA12	R15
49	GND	N/A	N/A	**50**	GND	N/A	N/A

**High drive outputs. An MCU signal feeds the high drive open collector darlington driver, which in turn outputs to the indicated header Pin#*

Table 10: I/O Header (HDR2)

Pin#	Signal	MCU Pin Name	MCU Pin Number	Pin#	Signal	MCU Pin Name	MCU Pin Number
1	GND	N/A	N/A	**2**	GND	N/A	N/A
3	3V3_VCC	N/A	N/A	**4**	5V0_VCC	N/A	N/A
5	VIN	N/A	N/A	**6**	VIN	N/A	N/A
7	ADC123_IN3	PA3	R2	**8**	ADC3_IN4	PF6	K2
9	ADC3_IN5	PF7	K1	**10**	ADC3_IN6	PF8	L3
11	ADC3_IN7	PF9	L2	**12**	ADC3_IN8	PF10	L1
13	ADC3_IN9	PF3	J2	**14**	ADC123_IN10	PC0	M2
15	ADC123_IN12	PC2	M4	**16**	ADC123_IN13	PC3	M5
17	ADC12_IN6	PA6	P3	**18**	ADC12_IN8	PB0	R5
19	ADC12_IN9	PB1	R4	**20**	DAC_OUT1	PA4	N4
21	DAC_OUT2	PA5	P4	**22**	GND	N/A	N/A
23	VDDA	N/A	R1	**24**	I2C2_SCL	PH4	H4
25	I2C2_SDA	PH5	J4	**26**	I2C2_SMBA	PH6	M11
27	I2C3_SCL	PH7	N12	**28**	I2C3_SDA	PH8	M12
29	I2C3_SMBA	PH9	M13	**30**	SPI1_SCK	PB3	A10
31	SPI1_MISO	PB4	A9	**32**	SPI1_MOSI	PB5	A6
33	SPI1_NSS	PA15	A13	**34**	PI11	PI11	E4
35	PI10	PI10	E3	**36**	PH2	PH2	F4
37	PH3	PH3	G4	**38**	USART1_TX	PB6	B6
39	USART1_RX	PB7	B5	**40**	USART6_CK	PG7	J14
41	USART6_TX	PC6	H15	**42**	USART6_RX	PG9	C10
43	USART6_CTS	PG15	B7	**44**	USART6_RTS	PG8	H14
45	PH13	PH13	E12	**46**	PI9	PI9	D3
47	WKUP	PA0	N3	**48**	RTC_TAMP/TS	PI8	D2
49	GND	N/A	N/A	**50**	GND	N/A	N/A

2.16 I2C

The MitiPy provides for two I2C hardware ports located on I/O header 2 (HDR2). Both can support a bit rate up to 100 kb/s (Standard mode) and 400 kb/s (Fast mode) with 7/10 bit addressing mode and a 7-bit addressing mode (as slave). By default, the I2C interface operates in Slave mode.

Table 11: I2C (HDR2)

Pin#	Port Line	Description
24	I2C2_SCL	I2C2 Clock signal
25	I2C2_SDA	I2C2 Data signal
26	I2C2_SMBA	I2C2 System Management Bus Alert signal
27	I2C3_SCL	I2C3 Clock signal
28	I2C3_SDA	I2C3 Data signal
29	I2C3_SMBA	I2C3 System Management Bus Alert signal

2.17 SPI

The MitiPy is equipped with one Serial Peripheral Interface bus communicating up to 42 Mbits/s. This provides for half/full duplex synchronous transfers with external devices with an 8 or 16-bit transfer frame format selection.

Table 12: SPI (HDR2)

Pin#	Port Line	Description
30	SPI1_SCK	SPI1 Serial Clock
31	SPI1_MISO	SPI1 Master In Slave Out
32	SPI1_MOSI	SPI1 Master Out Slave In
33	SPI1_NSS	SPI1 Slave Select

2.18 Analog to Digital Converter

The MitiPy has 13 A/D input channels with unique A/Ds available on the Utility I/O header 2 (HDR2). Voltages applied to the inputs must be in the range of 0 - 3.3V with reference to ground. For additional information please reference the STM32F407IGH6 User Manual. See Table 10 in the I/O Expansion section for pinout details.

2.19 Digital to Analog Converter

The MitiPy comes equipped with 2 D/A converters. These converters run directly from the ST Processor and are routed to I/O header HDR2. The output of the converters is 0V to 3.3V depending on digital count written to the D/A converter. For additional information please reference the STM32F407IGH6 User Manual. See Table 10 in the I/O Expansion section for pinout details.

2.20 Timers/Counters

The MitiPy is equipped with 25 timers and counters and are located on I/O header HDR1. TIM1 and TIM8 are advanced control timers that are 16-bit auto-reload counter driven by a programmable prescaler. TIM2 - TIM5 are general purpose timers that consist of 16-bit or 32-bit auto reload counter driven by a programmable prescaler. These timers can be used for generating output waveforms or for measuring pulse lengths of input signals and are completely independent and do not share any resources. See Table 9 in the I/O expansion section for pinout details.

2.21 Serial wire JTAG debug port (SWJ-DP)

The MitiPy provides a serial wire JTAG debug port (SWJ-DP) accessible through the MitiPy's cortex-m debug header (HDR3). The MCU's ARM SWJ-DP interface is embedded and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

After reset (SYSRESETn or PORESETn), all five pins used for the SWJ-DP are assigned as dedicated pins immediately usable by the debugger host (note that the trace outputs are not assigned except if explicitly programmed by the debugger host). However, the STM32F407 MCU offers the possibility of disabling some or all of the SWJ-DP ports and so, of releasing the associated pins for general-purpose (GPIO) usage.

Table 13: JTAG/SWD (HDR3)

Pin#	Signal	Description	MCU Pin Name	MCU Pin Number
1	3V3_VCC	3.3VDC	N/A	N/A
2	JTMS_SWDIO	JTAG Test Mode Selection	PA13	A15
3	GND	Ground	N/A	N/A
4	JTCK_SWCLK	JTAG Test Clock	PA14	A14
5	GND	Ground	N/A	N/A
6	JTDO_SWO	JTAG Test Data Output	PB3	A10
7	GND	Ground	N/A	N/A
8	JTDI	JTAG Test Data Input	PA15	A13
9	GND	Ground	N/A	N/A
10	SYS_RESET#	System Reset	NRST	J1

3 Software

The MitiPy offers the ability to use different operating systems to meet different customer needs. There are available board support packages for the MitiPy from EMAC that uses MicroPython and FreeRTOS. EMAC provides a fully functional MicroPython and FreeRTOS BSPs loaded on the MitiPy at no additional charge. Middleware has been added to compliment the already available middleware supplied by the developers at STM to make these packages available for easy integration into user developed applications targeted for the MitiPy.

3.1 MicroPython

MicroPython is one of the packages that is offered for the MitiPy. It is an implementation of the Python 3 programming language optimized to run on microcontrollers in a constrained environment. The MitiPy can be preloaded with the MicroPython BSP at no charge.

For more information on MicroPython support, please visit the EMAC Wiki MicroPython Section at:

http://wiki.emacinc.com/wiki/Micropython

3.1.1 Mu IDE

EMAC utilizes the Mu IDE for the MicroPython development which is a simple Python editor that is quick and easy to learn. The minimal setup makes it easy to use so the user can jump right in to developing. It has a built in REPL (Read Evaluate Print Loop) console window for easy command input and debugging.

https://codewith.mu/en/

3.2 FreeRTOS

FreeRTOS is one of the many packages available for application development that can be included when using the STM32CubeIDE code generation tool. Optionally, the FreeRTOS package can be downloaded from https://www.freertos.org/. FreeRTOS has their own board support package for many of the available STM32 development platforms. When using the STM32CubeIDE code generator, a wrapper is provided for most of the FreeRTOS functionality to make development even more simple.

https://www.freertos.org/FreeRTOS-Plus/BSP_Solutions/ST/index.html

Amazon provides Amazon Web Services (AWS) cloud support for FreeRTOS. For further information go to: https://aws.amazon.com/freertos/getting-started/

3.2.1 STM32CubeIDE

EMAC utilizes the STM32CubeIDE all-in-one multi OS development tool which is an advanced C/C++ development platform with IP configuration, code generation, code compilation, and debug features for STM32 microcontrollers. The ST32CubeIDE integrates all STM32CubeMX functionalities to offer an all-in-one tool experience while saving installation and development time. The MitiPy board support package includes the STM32CubeIDE project that can be used to tailor the FreeRTOS build to the customer's exact needs.

https://www.st.com/en/development-tools/stm32cubeide.html

3.2.1.1 STM32CubeMX

The STM32CubeMX is used to configure the processor for the MitiPy board. This tool allows for the configuration of all processor pins as well as adding, removing, and configuring middleware packages that are available through the STM32CubeMX code generation tool. One of the benefits of using the code generation tool is that it will automatically pull in and use the most current software updates from the upstream repository. Some of the middleware packages that are available and are supported by the MitiPy are as follows;

- FatFS
- FreeRTOS
- LwIP
- MBEDTLS
- USB Device
- USB Host
- Redpine APIs

http://www.st.com/en/development-tools/stm32cubemx.html

3.2.1.2 STM32CubeMX Expansion Software

Additional software and expansion packs are available through STMicro for use with the STM32CubeMX code generation utility. Software expansion packs may need to be tailored specifically to work with the MitiPy board, however, they are a useful starting point for incorporating various sensors and peripherals to the MitiPy board.

http://www.st.com/en/ecosystems/stm32cube-expansion-software.html?querycriteria=productId=SC2005

4 Appendix A: Connector Pinouts

4.1 Serial Port COM A (CN1)

Pin	DB9 Connector: Description
1	NC
2	RXD
3	TXD
4	NC
5	GND
6	NC
7	RTS
8	CTS
9	NC

4.2 I/O Header (HDR1)

Pin#	Signal	MCU Pin Name	MCU Pin Number	Pin#	Signal	MCU Pin Name	MCU Pin Number
1	GND	N/A	N/A	**2**	GND	N/A	N/A
3	3V3_VCC	N/A	N/A	**4**	5V0_VCC	N/A	N/A
5	VIN	N/A	N/A	**6**	V_HIDRV	N/A	N/A
7	TIM1_ETR	PE7	R8	**8**	TIM1_CH1N	PE8	P8
9	TIM1_CH1	PE9	P9	**10**	TIM1_CH2N	PE10	R9
11	TIM1_CH2	PE11	P10	**12**	TIM1_CH3N	PE12	R10
13	TIM1_CH3	PE13	N11	**14**	TIM1_CH4	PE14	P11
15	TIM1_BKIN	PE15	R11	**16**	TIM2_CH3	PB10	R12
17	TIM2_CH4	PB11	R13	**18**	TIM3_CH2	PC7	G15
19	TIM4_CH2	PD13	M15	**20**	TIM4_ETR	PE0	A4
21	TIM4_CH3	PD14	M14	**22**	GND	N/A	N/A
23	TIM5_CH1	PH10	L13	**24**	TIM4_CH4	PD15	L14
25	TIM5_CH3	PH12	K12	**26**	TIM5_CH2	PH11	L12
27	TIM8_CH3N	PH15	D13	**28**	TIM8_CH2N	PH14	E13
29	TIM8_CH1	PI5	C4	**30**	TIM8_BKIN	PI4	D4
31	TIM8_CH3	PI7	C2	**32**	TIM8_CH2	PI6	C3
33*	HD_PG1	PG1	M7	**34***	HD_PG0	PG0	N7
35*	HD_PG3	PG3	K15	**36***	HD_PG2	PG2	L15
37*	HD_PG5	PG5	K13	**38***	HD_PG4	PG4	K14
39*	HD_PG10	PG10	B10	**40***	HD_PG6	PG6	J15
41	PF12	PF12	P6	**42**	PF13	PF13	N6
43	PF14	PF14	R7	**44**	PF15	PF15	P7
45	OTG_HS_ID	PB12	P12	**46**	OTG_HS_VBU	PB13	P13
47	OTG_HS_DM	PA11	R14	**48**	OTG_HS_DP	PA12	R15
49	GND	N/A	N/A	**50**	GND	N/A	N/A

4.3 I/O Header (HDR2)

Pin#	Signal	MCU Pin Name	MCU Pin Number	Pin#	Signal	MCU Pin Name	MCU Pin Number
1	GND	N/A	N/A	**2**	GND	N/A	N/A
3	3V3_VCC	N/A	N/A	**4**	5V0_VCC	N/A	N/A
5	VIN	N/A	N/A	**6**	VIN	N/A	N/A
7	ADC123_IN3	PA3	R2	**8**	ADC3_IN4	PF6	K2
9	ADC3_IN5	PF7	K1	**10**	ADC3_IN6	PF8	L3
11	ADC3_IN7	PF9	L2	**12**	ADC3_IN8	PF10	L1
13	ADC3_IN9	PF3	J2	**14**	ADC123_IN10	PC0	M2
15	ADC123_IN12	PC2	M4	**16**	ADC123_IN13	PC3	M5
17	ADC12_IN6	PA6	P3	**18**	ADC12_IN8	PB0	R5
19	ADC12_IN9	PB1	R4	**20**	DAC_OUT1	PA4	N4
21	DAC_OUT2	PA5	P4	**22**	GND	N/A	N/A
23	VDDA	N/A	R1	**24**	I2C2_SCL	PH4	H4
25	I2C2_SDA	PH5	J4	**26**	I2C2_SMBA	PH6	M11
27	I2C3_SCL	PH7	N12	**28**	I2C3_SDA	PH8	M12
29	I2C3_SMBA	PH9	M13	**30**	SPI1_SCK	PB3	A10
31	SPI1_MISO	PB4	A9	**32**	SPI1_MOSI	PB5	A6
33	SPI1_NSS	PA15	A13	**34**	PI11	PI11	E4
35	PI10	PI10	E3	**36**	PH2	PH2	F4
37	PH3	PH3	G4	**38**	USART1_TX	PB6	B6
39	USART1_RX	PB7	B5	**40**	USART6_CK	PG7	J14
41	USART6_TX	PC6	H15	**42**	USART6_RX	PG9	C10
43	USART6_CTS	PG15	B7	**44**	USART6_RTS	PG8	H14
45	PH13	PH13	E12	**46**	PI9	PI9	D3
47	WKUP	PA0	N3	**48**	RTC_TAMP/TS	PI8	D2
49	GND	N/A	N/A	**50**	GND	N/A	N/A

4.4 Serial Wire JTAG Debug Port (HDR3)

Pin#	Port Line	Description
1	3V3_VCC	3.3VDC
2	JTMS_SWDIO	JTAG Test Mode Selection, SW Data Input / Output
3	GND	Ground
4	JTCK_SWCLK	JTAG Test Clock, SW Clock
5	GND	Ground
6	JTDO_SWO	JTAG Test Data Output, TRACESWO
7	GND	Ground
8	JTDI	JTAG Test Data Input
9	GND	Ground
10	SYS_RESET#	System Reset

4.5 CAN 2.0 Port (HDR4)

Pin	Signal
1	CAN_H
2	CAN_L
3	GND

4.6 Serial Port COM B (HDR5)

Pin	10-Pin Header: Description (RS-232)	10-Pin Header Description (RS-485/422)
1	NC	TX-
2	NC	NC
3	RXD	TX+
4	RTS	NC
5	TXD	RX+
6	CTS	NC
7	NC	RX-
8	NC	NC
9	GND	GND
10	NC	NC

4.7 MultiConnect mDot Serial Wire Debug Port (HDR9)

Pin#	Port Line	Description
1	3V3_VCC	3.3VDC, mDot_Vout
2	JTMS_SWDIO	Serial Wire Data Input / Output
3	GND	Ground
4	JTCK_SWCLK	Serial Wire Clock
5	GND	Ground
6	JTDO_SWO	TRACESWO
7	GND	Ground
8	NC	No Connect
9	GND	Ground
10	SYS_RESET#	mDot Serial Wire Reset

4.8 Module Socket (SOK2)

Pin#	Signal	Pin#	Signal
1	VDD	**2**	USART6_RX
3	USART6_TX	**4**	GND
5	SKY_RST#	**6**	SKY_VUSB
7	SKY_USB+	**8**	SKY_USB-
9	USART6_DTR	**10**	GND
11	GND	**12**	USART6_CTS
13	SKY_STAT	**14**	3V3_VCC
15	GND	**16**	USART6_RTS
17	NC	**18**	NC
19	NC	**20**	SKY_ON-OFF

4.9 Module Socket (SOK3)

Pin#	Signal	Pin#	Signal
1	VDD	**2**	USART1_RX
3	USART1_TX	**4**	XBee_MISO
5	RAD_RST#	**6**	NC
7	NC	**8**	NC
9	NC	**10**	GND
11	XBee_MOSI	**12**	NC
13	NC	**14**	NC
15	NC	**16**	NC
17	XBee_SNSS	**18**	XBee_SCK
19	NC	**20**	NC
24	mDOT_VOUT	**25**	GND
26	mDOT_SWCLK	**27**	mDOT_SWDIO
28	mDOT_JRST	**29**	mDOT_SWO
30	NC	**31**	NC

4.10 Power Supply Terminal Block (ST1)

Pin	Signal
1	Vin
2	GND
3	Chassis GND

5 Appendix B: Jumper Settings

5.1 JB1 (Boot Mode 0 Selection)

Jumper	Position	Setting
Pins 1 & 2	RXM	Select RXM
Pins 2 & 3*	FLS	Select FLS

*Default Setting

5.2 JB2 (Boot Mode 1 Selection)

Jumper	Position	Setting
Pins 1 & 2	RAM	Select RAM
Pins 2 & 3*	ROM	Select ROM

*Default Setting

When JB1 is in the RXM position and JB2 is in the ROM position the system will Boot from the ST bootloader. This bootloader will allow the programming of the Main Flash Memory by a number of various serial peripherals (USART, CAN, USB, I2C, SPI, etc.). Care must be exercised when using this jumper option as any program currently in Flash can be erased or corrupted. For additional information please reference the STM32F407IGH6 User Manual.

5.3 JB3 (RTC & RAM Retention Battery)

Jumper	Position	Setting
Pins 1 & 2	ON	Enable Battery
Pins 2 & 3*	OFF	Disable Battery

*Default Setting

5.4 JB4 (CAN Termination)

Jumper	Position	Setting
Pins 1 & 2	TRM	Termination
Pins 2 & 3*	OFF	No Termination

*Default Setting

5.5 JB5 (SOK2 Power Supply Voltage Option)

Jumper	Position	Setting
Pins 1 & 2*	3V3	3.3VDC Supply Voltage
Pins 2 & 3	3V8	3.8VDC Supply Voltage

*Default Setting

5.6 JB6 (SOK3 Power Supply Voltage Option)

Jumper	Position	Setting
Pins 1 & 2*	3V3	3.3VDC Supply Voltage
Pins 2 & 3	5V0	5.0VDC Supply Voltage

*Default Setting

6 Appendix C: Dimensional Drawing