SoM-iMX6U

User Manual

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Revision 1.20

(for use with Rev 2 boards or newer)

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1 Introduction

This document describes EMAC's SoM-iMX6U System-on-Module (SoM). The SoM-iMX6U is designed to be compatible with EMAC's 144-pin SODIMM form factor. This module is built around the Freescale/NXP i.MX 6UltraLite (MCIMX6G1) Cortex A7 528MHz processor, which provides several of its key features.

The SoM-iMX6U has onboard Ethernet PHY, 5 serial ports, 2 USB 2.0 ports, 1 I2S audio port, 1 SDIO SD port, 1 I2C port, 2 CAN port, an internal real time clock (RTC), a programmable clock synthesizer, onboard eMMC flash, a Serial NOR Flash and LPDDR2 RAM.

In addition to the standard SoM features, the SoM-iMX6U also features a fast 32-bit core, open source software support, and a wide range of controller I/O pins.

1.1 Features

- **Small, 144 pin SODIMM form factor (2.66" x 1.5")**
- **NXP ARM Cortex-A7 MCIMX6G1CVM05AA 528MHz Processor**
- **10/100 BaseT Ethernet with on-board PHY**
- **16-bit External Bus Interface**
- **4 Serial RS232 ports and 1 Serial RS232/422/485 port**
- **2 USB 2.0 (High Speed) OTG ports**
- **512/128 MB LPDDR2**
- **4 GB of Resident eMMC Flash**
- **16 MB of Serial Data Flash**
- **Battery-backed Real-Time Clock**
- **SD/MMC Flash Card Interface**
- **1 SPI port**
- **1 I2C port**
- **1 I2S Audio port**
- **2 CAN Bus Interface**
- **Timer/Counters and Pulse Width Modulation (PWM) ports**
- **4-Channel 12-bit Analog-to-Digital Converter**
- **Typical power requirement: 3.3V @ 170 mA**
- **JTAG for debug, including real-time trace**
- **FREE QT Creator IDE with GCC and GDB development tools**

2 Hardware

2.1 Specifications

- **CPU:** Embedded NXP MCIMX6G1CVM05AA processor running at 528 MHz
- **Flash:** 4 GB eMMC Flash and 16 MB of Serial NOR Flash
- **RAM:** 512/128 MB LPDDR2
- **Flash Disk:** 4-bit Parallel or SPI serial SDHC/MMC interface
- **System Reset:** Supervisor with external Reset Button provision
- **RTC:** Real-Time Clock with battery-backed provision using 32-bit free running counter
- **Timer/Counters:** 2, 3-channel , 32-bit timers/counters with capture, compare, and PWM
- **Watchdog Timer:** External Watchdog Timer (MAX6747)
- **Digital I/O:** 18 General Purpose I/Os with 16mA drive when used as an output
- **Analog I/O:** 4-channel, 12-bit Analog-to-Digital Converter (ADC)
- **Power:** Power Management Controller allows selectively shutting down on-processor I/O functionality and running from a slow clock
- **JTAG:** JTAG for debug, including real-time trace
- **Clocks:** PLL synthesized 8 MHz, 200 KHz, and 14.3 MHz clock outputs

Serial Interfaces

- **UARTS:** 4 Serial RS232 ports with no handshaking and 1 Serial RS232/422/485 port with handshaking
- **SPI:** 1 High-Speed SPI port with chip select
- **Audio:** I2S Synchronous Serial Controller with Analog interface support
- **USB:** 2 USB 2.0 High-Speed OTG ports

Ethernet Interface

- **MAC:** MCIMX6G1CVM05AA on chip MAC
- **PHY:** Micrel KSZ8081 low power PHY with software shutdown and slow clock modes
- **Interface:** IEEE 802.3u 10/100 BaseT Fast Ethernet (requires external magnetics and Jack)

Bus Interface:

- Local ARM MCIMX6G1CVM05AA Bus accessible through SODIMM provides 8 address lines, 16 data bus lines, and control lines.

Mechanical and Environmental

- **Dimensions:** SODIMM form factor with the length dimension extended (2.66" x 1.5")
- **Power Supply Voltage:** +3.3 Volts DC +/- 5%
- **Power Requirements (typical):**
  - Typical 3.3 Volts @ 300mA (0.56 watts)
  - Max current draw during boot process: 300 mA
  - Constant busy loop: 240 mA
  - Idle system: 170 mA
  - APM sleep mode with Ethernet PHY disabled: 3.60 mA
- **Operating Temperature:** -40 ~ 85° C (-40 ~ 185 ° F), fan-less operation
- **Operating Humidity:** 0% ~ 90% relative humidity, non-condensing

2.2 Real-Time Clock

The SoM-iMX6U has an embedded Real-time Clock. Battery backup is provided from the carrier board using the VSTBY pin. The SoM-iMX6U will retain the RTT value register during reset and hence use it as a RTC. The RTC has the provision to set alarms that can interrupt the processor. For example, the processor can be placed in sleep mode and then later awakened using the alarm function.

2.3 Watchdog Timer

The SoM-iMX6U provides an external Watchdog Timer/ Supervisor (MAX6747) with an extended watchdog timeout period of 1.42 seconds (±10%). Upon power-up the Watchdog is disabled and does not require pulsing. To start the Watchdog, it must first be enabled. This is done by configuring port line CSI_HSYNC as an output and setting it low in software. Once enabled, the Watchdog should be pulsed, using port line LCD_DATA02, continually every 1.28 seconds or faster to prevent the Watchdog from timing out and resetting the module. If the user is using the watchdog to force a system reset, the watchdog may need up to 1.56 seconds of inactivity before the watchdog reset will occur. The watchdog is automatically disabled upon reset but it can also be disabled by setting CSI_HSYNC high.

2.4 External Connections

The SoM-iMX6U connects to a carrier board containing its connectors, power supply and any expansion I/O, through a standard ENIG-plated (Electroless Nickel Immersion Gold) SODIMM 144 pin connection (top half shown below).

The SoM model will fit in any standard 144-pin SODIMM socket. These connections are designed to be compatible with all EMAC 144-pin SoM products. See EMAC SoM 144-pin SODIMM pin-out Specification to see how other 144-pin SoMs pin-outs line up with the SoM-iMX6U's pin-out.

The use of the SODIMM form-factor for EMAC's SoMs is a sound choice that has been proven rugged and reliable in the laptop market.

2.4.1 External Bus

Table 1: External Bus

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
100	GP_CS1	CSI_MCLK/EIM_CS0#	GPIO4_IO17	General Purpose Processor Chip Select CS0
98	GP_CS2	NAND_READY/EIM_CS1#	GPIO4_IO12	General Purpose Processor Chip Select CS1
108	GP_CS3	LCD_CLK/EIM_CS2#	GPIO3_IO00	General Purpose Processor Chip Select CS2
16	~RD/~OE	CSI_PIXCLK/EIM_OE	GPIO4_IO18	Read Signal
83	~WR	CSI_SYNC/EIM_RW	GPIO4_IO19	Write Signal
6	~RST_IN	POR	N/A	Processor Reset
43	~RST_OU	POR	N/A	Processor Reset
85	Flash WP	FLASH_WP# (N25Q064)	N/C	Serial Flash Write Protect
72	ALE/~TS	SNVS_PMIC_ON_REQ	N/A	External PMIC Enable
26	A0	CSI_DATA00/EIM_AD0	GPIO4_IO21	Address Bus
35	A1	CSI_DATA01/EIM_AD1	GPIO4_IO22	Address Bus
33	A2	CSI_DATA02/EIM_AD2	GPIO4_IO23	Address Bus
31	A3	CSI_DATA03/EIM_AD3	GPIO4_IO24	Address Bus
28	A4	CSI_DATA04/EIM_AD4	GPIO4_IO25	Address Bus
109	A5	CSI_DATA05/EIM_AD5	GPIO4_IO26	Address Bus
111	A6	CSI_DATA06/EIM_AD6	GPIO4_IO27	Address Bus
113	A7	CSI_DATA07/EIM_AD7	GPIO4_IO28	Address Bus
10, 12, 18, 14, 37, 5, 11, 9, 7, 13, 97, 17, 15, 104	A8-A21	N/C		
29	D0	LCD_DATA08/EIM_DATA	GPIO3_IO13	Data Bus
27	D1	LCD_DATA09/EIM_DATA	GPIO3_IO14	Data Bus
25	D2	LCD_DATA10/EIM_DATA	GPIO3_IO15	Data Bus
22	D3	LCD_DATA11/EIM_DATA	GPIO3_IO16	Data Bus
23	D4	LCD_DATA12/EIM_DATA	GPIO3_IO17	Data Bus
21	D5	LCD_DATA13/EIM_DATA	GPIO3_IO18	Data Bus
19	D6	LCD_DATA14/EIM_DATA	GPIO3_IO19	Data Bus
20	D7	LCD_DATA15/EIM_DATA	GPIO3_IO20	Data Bus
8	D8	LCD_DATA16/EIM_DATA	GPIO3_IO21	Data Bus
24	D9	LCD_DATA17/EIM_DATA	GPIO3_IO22	Data Bus
34	D10	LCD_DATA18/EIM_DATA	GPIO3_IO23	Data Bus
70	D11	LCD_DATA19/EIM_DATA	GPIO3_IO24	Data Bus
77	D12	LCD_DATA20/EIM_DATA	GPIO3_IO25	Data Bus
81	D13	LCD_DATA21/EIM_DATA	GPIO3_IO26	Data Bus
84	D14	LCD_DATA22/EIM_DATA	GPIO3_IO27	Data Bus
86	D15	LCD_DATA23/EIM_DATA	GPIO3_IO28	Data Bus

2.4.2 JTAG

The SoM specification allows for access to the JTAG lines for the MCIMX6G1CVM05AA processor. These connections are shared with the I2S interface; as such installation of jumper resistors as well as custom software will need to be deployed to enable the JTAG lines' capability to debug software.

Table 2: Processor JTAG

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
139	JTAG_TCK	JTAG_TCK (Optional)	GPIO1_IO14	JTAG clock
137	JTAG_TDI	JTAG_TDI (Optional)	GPIO1_IO13	JTAG serial in
138	JTAG_TDO	JTAG_TDO (Optional)	GPIO1_IO12	JTAG serial out
140	JTAG_TMS	JTAG_TMS (Optional)	GPIO1_IO11	JTAG operation mode
112	JTAG_TRST	JTAG_TRST (Optional)	GPIO1_IO15	Test Reset Signal

2.4.3 One-Wire / I2C

The SoM specification calls for a one-wire port. Since the SoM-iMX6U does not have a one-wire port, this line is not connected for One-Wire Operation. The MCIMX6G1CVM05AA processor does provide an I2C bus and so these pins are dedicated to that function although they can also be used as GPIOs. The I2C bus lines have 4.7K Ohm pull up resistors installed on the SoM-iMX6U.

Table 3: One-Wire / I2C Port

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
116	LOCAL1W/SCL	GPIO1_IO02/I2C1_SCL	GPIO1_IO02	I2C Clock
88	SDA	GPIO1_IO03/I2C1_SDA	GPIO1_IO03	I2C Data

2.4.4 Ethernet

The SoM-iMX6U provides a Micrel KSZ8081 Low Power Ethernet RMII PHY IC on board. Carrier designers need only run these lines through the appropriate magnetics layer to have a functional Ethernet connection. Remember the RX and TX lines are differential pairs and need to be routed as such.

The LED/configuration pins' state at reset determines the Ethernet's configuration (10-baseT, 100-baseT, autoconfig) and the function of the LED's. The SoM-100ES and the SoM-150ES pull them all high, which configures the chip for network autoconfig, with LED0 functioning as active low link, and LED1 is functioning as active low Rx Activity (Refer to Carrier schematics).

The Ethernet PHY can be put into a low power mode by writing directly to the MAC via software. The PHY clock is automatically turned off to conserve power when the SoM is put into sleep mode.

Table 4: Ethernet

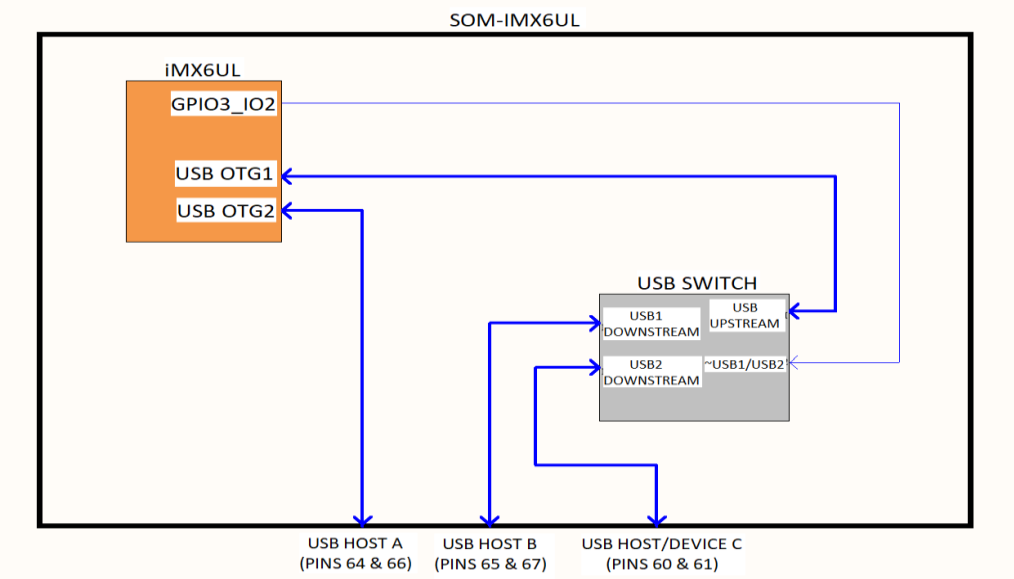
SODIMM Pin#	SoM Pin Name	{PHY} Pin Name	Port Line	Description
89	LED_LINK/CFG_1	LED0/NWAYEN (KSZ8081)	N/A	Ethernet Link LED Configuration Pin
90	LED_RX/CFG_2	LED1/SPEED (KSZ8081)	N/A	Ethernet Activity LED Configuration pin
94	Ethernet_Rx-	RXM (KSZ8081)	N/A	Low differential Ethernet receive line
92	Ethernet_Rx+	RXP (KSZ8081)	N/A	High differential Ethernet receive line
93	Ethernet_Tx-	TXN (KSZ8081)	N/A	Low differential Ethernet transmit line
91	Ethernet_Tx+	TXP (KSZ8081)	N/A	High differential Ethernet transmit line

2.4.5 USB

The SoM-iMX6U provides 2 High speed USB 2.0 Host/Device ports. Both USB ports can be used as OTG by making use of the alternative pin functions of various IOs on the SoM-iMX6U. The SoM-iMX6U makes use of an onboard USB switch to route OTG1 port to either USB Host B or the USB Device C pins on the card edge. This is done to maintain compatibility with existing EMAC products. The Device/Host port connects to a USB Type B connector on the SoM-100ES, SoM-112ES, and SoM-150ES carrier boards.

To switch OTG1 bus routing between the host and device port the GPIO3_IO2 pin can be toggled. By default the processor pin is set to high upon boot to facilitate programming through the USB device interface. The OTG1 port lines can be routed to the host card edge connections by writing GPIO3_IO2 low. See block diagram below.

USB Block Diagram



OTG1_ID can be accessed through SoM pin 40, OTG1_PWR can be accessed through SoM pin 117, and OTG1_OC can be accessed through SoM pin 105 for custom carriers that make use of true OTG functionality. For low power applications the lowest power can be achieved by leaving the USB switch control line in the high (default) state.

Table 5: USB

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
64	USB Host A+	USB_OTG2_DP	N/A	Host, High Speed USB 2
66	USB Host A-	USB_OTG2_DN	N/A	Host, High Speed USB 2
60	USB Device C-	HSD2- (FSUSB43L10x)	N/C	Device/Host, HS USB 1
61	USB Device C+	HSD2+ (FSUSB43L10x)	N/C	Device/Host, HS USB 1
45	Vbus	N/C	N/C	USB OTG VBUS Detect
65	USB Host B+	HSD1+ (FSUSB43L10x)	N/C	Device/Host, HS USB 1
67	USB Host B-	HSD1- (FSUSB43L10x)	N/C	Device/Host, HS USB 1
40	GPIO0	GPIO1_IO00/OTG1_ID	GPIO1_IO00	GPIO 0
117	GPIO3	GPIO1_IO04/OTG1_PWR	GPIO1_IO04	GPIO 3
105	GPIO13	GPIO1_IO01/OTG1_OC	GPIO1_IO01	GPIO 13

2.4.6 SPI

The MCIMX6G1CVM05AA processor provides a dual (SPI3 and SPI4) SPI module for communicating with peripheral devices. On the SoM the SPI4 bus is already connected to the serial flash, which uses SPI4_CS0# (SPI4_CS0# is not brought out to the card fingers). The first Table below lists the lines for the #4 SPI module. The SoM pin specification allows for three SPI chip selects. The SPI chip selects available to the card edge are SPI_CS0, SPI_CS1, and SPI_CS2. The second Table below lists the lines for the SPI3 module.

Table 6: Serial Peripheral Interface

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
122	SPI_MI	ENET2_TX_CLK/SPI4_MISO	GPIO2_IO14	SPIO4 serial data in
121	SPI_MO	ENET2_TX_EN/SPI4_MOSI	GPIO2_IO13	SPIO4 serial data out
120	SPI__SCK	ENET2_TX_DATA1/SPI4_SCLK	GPIO2_IO12	SPIO4 serial clock out
123	SPI_CS0	ENET2_RX_EN	GPIO2_IO10	SPIO4 slave select line 0
124	SPI_CS1	ENET2_TX_DATA0	GPIO2_IO11	SPIO4 slave select line 1
110	SPI_CS2	LCD_DATA04	GPIO3_IO09	SPIO4 slave select line 2

Table 7: Serial Peripheral Interface 3

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port line	Description
133	GPIO9	NAND_CLE/SPI3_MISO	GPIO4_IO15	SPIO3 serial data in/GPIO
134	GPIO10	NAND_CE1#/SPI3_MOSI	GPIO4_IO14	SPIO3 serial data out/GPIO
135	GPIO11	NAND_CE0#/SPI3_SCLK	GPIO4_IO13	SPIO3 serial clock out/GPIO
136	GPIO12	NAND_ALE/SPI3_CS1#	GPIO4_IO10	SPIO3 slave select line 0/GPIO
105	GPIO13	GPIO1_IO01/OTG1_OC	GPIO1_IO01	SPIO3 slave select line 1/GPIO

2.4.7 MCI Multimedia Card / SDIO

The MCIMX6G1CVM05AA processor provides a 4-bit MMC/SD card interface using the MC lines. The SoM-100ES Carrier board uses a serial SPI based MMC/SD interface. The SoM-iMX6U could be programmed to use this serial interface, however the drivers provided are written to utilize the 4-bit interface and as such require the SoM-150ES Carrier board to use these drivers.

Table 8: MMC/SD Card Interface

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
54	MMC/SD 4-Bit CLK	NAND_RE#/SD2_CLK	GPIO4_IO00	SD Clock
51	MMC/SD 4-Bit CMD	NAND_WE#/SD2_CMD	GPIO4_IO01	SD Command
50	MMC/SD 4-Bit DA0	NAND_DATA00/SD2_DATA0	GPIO4_IO02	SD Data 0
55	MMC/SD 4-Bit DA1	NAND_DATA01/SD2_DATA1	GPIO4_IO03	SD Data 1
56	MMC/SD 4-Bit DA2	NAND_DATA02/SD2_DATA2	GPIO4_IO04	SD Data 2
57	MMC/SD 4-Bit DA3	NAND_DATA03/SD2_DATA3	GPIO4_IO05	SD Data 3
42	SD_Card_Detect	NAND_WP#	GPIO4_IO11	SD Card Detect

2.4.8 Serial Ports

The SoM-144 pin specification has the provision for 4 serial ports. However, the MCIMX6G1CVM05AA provides 5 serial ports so the 2 additional serial ports are accommodated through the use of alternate SoM pins.

Table 9: Serial Ports

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
71	COMA_RXD	UART3_RX_DATA	GPIO1_IO25	UART3 Receive/GPIO
73	COMA_TXD	UART3_TX_DATA	GPIO1_IO24	UART3 Transmit/GPIO
38	COMB_RXD	UART2_RX_DATA	GPIO1_IO21	UART2 Receive/GPIO
36	COMB_TXD	UART2_TX_DATA	GPIO1_IO20	UART2 Transmit/GPIO
82	COMB_RTS/GPIO	UART2_CTS_B	GPIO1_IO22	UART2 CTS/GPIO
78	COMB_CTS/GPIO	UART2_RTS_B	GPIO1_IO23	UART2 RTS/GPIO
103	COMC_RXD	UART1_RX_DATA	GPIO1_IO17	UART1 Receive/GPIO
102	COMC_TXD	UART1_TX_DATA	GPIO1_IO16	UART1 Transmit/GPIO
107	COMC_DSR/GPIO	NAND_DATA05	GPIO4_IO07	UART1 DSR /GPIO
106	COMC_DTR/GPIO	NAND_DATA06	GPIO4_IO08	UART1 DTR/GPIO
76	COMC_RI/GPIO	NAND_DATA07	GPIO4_IO09	UART1 RING/GPIO
30	COMC_DCD/GPIO	NAND_DATA04	GPIO4_IO06	UART1 DCD/GPIO
39	COMC_RTS/GPIO	UART1_CTS_B	GPIO1_IO18	UART1 CTS/GPIO
79	COMC_CTS/GPIO	UART1_RTS_B	GPIO1_IO19	UART1 RTS/GPIO
46	COME RX	UART5_RX_DATA	GPIO1_IO31	Debug Receive / GPIO
47	COME TX	UART5_TX_DATA	GPIO1_IO30	Debug Transmit / GPIO
49	COMD RX	UART4_RX_DATA	GPIO1_IO29	UART4 Receive / GPIO
48	COMD TX	UART4_TX_DATA	GPIO1_IO28	UART4 Transmit / GPIO

2.4.9 I2S

The SoM-iMX6U provides an I2S serial interface for connecting to an audio codec. These lines are shared with the processor's JTAG lines although the default functionality is I2S. To employ JTAG functionality see section 2.4.2 JTAG.

Table 10: I2S

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
87	Audio SCLK	JTAG_TDI/I2S2_BCLK	GPIO1_IO13	Transmit Clock/GPIO
80	Audio LRCK/TF	JTAG_TDO/I2S2_SYNC	GPIO1_IO12	Transmit Frame / GPIO
125	Audio SDIN	JTAG_TRST/I2S2_TXD	GPIO1_IO15	Serial Receive Data / GPIO
126	Audio SDOUT	JTAG_TCK/I2S2_RXD	GPIO4_IO14	Serial Transmit Data / GPIO
128	Audio RF	JTAG_TMS/I2S2_MCLK	GPIO1_IO11	Receive Frame / GPIO
127	GPIO4	GPIO1_IO05/OTG2_ID	GPIO1_IO05	Receive Clock / GPIO

2.4.10 CAN

The MCIMX6G1CVM05AA has two CAN controllers that are brought out to the SoM card edge. One is defined by the SoM specification and the second can be utilized instead of the serial port COM B control lines. The SoM specified CAN port can be used as GPIO if desired.

Table 11: CAN

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
96	CANTX	UART3_CTS_B/CAN1_TX	GPIO1_IO26	CAN Transmit / GPIO
95	CANRX	UART3_RTS_B/CAN1_RX	GPIO1_IO27	CAN Receive / GPIO

Table 12: Additional CAN Port

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
78	COMB_CTS/GPIO	UART2_RTS_B	GPIO1_IO23	CAN Receive / UART2 CTS
82	COMB_RTS/GPIO	UART2_CTS_B	GPIO1_IO22	CAN Transmit / UART2 RTS

2.4.11 GPIO

This section provides for the SoM general purpose IO section (GPIO). All of these pins can be configured to be general-purpose digital ports. These pins often have other capabilities besides GPIO as well but be aware that these additional capabilities cannot always be guaranteed to be shared between different pin-compatible EMAC SoMs.

Interrupts:

The MCIMX6G1CVM05AA is capable of using any GPIO pin as an interrupt as well as the pins that are labeled IRQ. The 144-Pin SoM Specification defines 3 IRQs.

Table 13: Interrupt Lines

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
75	GPIO1	LCD_VSYNC	GPIO3_IO03	Interrupt A / GPIO 1
32	GPIO2	LCD_RESET	GPIO3_IO04	Interrupt B / GPIO 2
40	GPIO0	GPIO1_IO00/OTG1_ID	GPIO1_IO00	Interrupt C / GPIO 0

A/D:

The MCIMX6G1CVM05AA Analog to Digital pins provides 4 channels of 12-bit resolution with a 1 us conversion time. With the enhanced DSP extensions, this can make quite a capable signal processor. The Analog to Digital Reference Voltage is enabled by default, but can be controlled by LCD_ENABLE pin of the processor. LCD_ENABLE pin configured as an input disables the reference, or it can be enabled by configuring it as an output and driving it low. For low power applications the least power is used when the ADC voltage reference is left off.

Table 14: Analog to Digital Converters

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
129	GPIO5	GPIO1_IO06/ADC_IN6	GPIO1_IO06	ADC CH1 / GPIO 5
130	GPIO6	GPIO1_IO07/ADC_IN7	GPIO1_IO07	ADC CH2 / GPIO 6
131	GPIO7	GPIO1_IO08/ADC_IN8	GPIO1_IO08	ADC CH3 / GPIO 7
132	GPIO8	GPIO1_IO09/ADC_IN9	GPIO1_IO09	ADC CH4 / GPIO 8

Timer/Counters:

The general-purpose Timer/Counter (TC) module on the MCIMX6G1CVM05AA is comprised of six 32-bit timer/counter channels with independently programmable input capture or output compare lines. These can be used for a wide variety of timed applications, including counters and PWM.

Table 15: Timers/Counters

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
117	GPIO3	GPIO1_IO04/OTG1_PWR	GPIO1_IO04	Programmable Clock / GPIO 3
127	GPIO4	GPIO1_IO05/OTG2_ID	GPIO1_IO05	Programmable Clock / GPIO 4
114	GPIO14	LCD_DATA00/PWM1_OUT	GPIO3_IO05	PWM / Clock / GPIO 14
115	GPIO15	LCD_DATA01/PWM2_OUT	GPIO3_IO06	PWM / Clock / GPIO 15

GPIOs:

Table 16: General Purpose IO

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
40	GPIO0	GPIO1_IO00/OTG1_ID	GPIO1_IO00	Interrupt C / GPIO 0
75	GPIO1	LCD_VSYNC	GPIO3_IO03	Interrupt A / GPIO 1
32	GPIO2	LCD_RESET	GPIO3_IO04	Interrupt B / GPIO 2
117	GPIO3	GPIO1_IO04/OTG1_PWR	GPIO1_IO04	Programmable Clock / GPIO 3
127	GPIO4	GPIO1_IO05/OTG2_ID	GPIO1_IO05	Programmable Clock / GPIO 4
129	GPIO5	GPIO1_IO06/ADC_IN6	GPIO1_IO06	ADC CH1 / GPIO 5
130	GPIO6	GPIO1_IO07/ADC_IN7	GPIO1_IO07	ADC CH2 / GPIO 6
131	GPIO7	GPIO1_IO08/ADC_IN8	GPIO1_IO08	ADC CH3 / GPIO 7
132	GPIO8	GPIO1_IO09/ADC_IN9	GPIO1_IO09	ADC CH4 / GPIO 8
133	GPIO9	NAND_CLE/SPI3_MISO	GPIO4_IO15	SPI3 Master In / GPIO 9
134	GPIO10	NAND_CE1#/SPI3_MOSI	GPIO4_IO14	SPI3 Master Out / GPIO 10
135	GPIO11	NAND_CE0#/SPI3_SCLK	GPIO4_IO13	SPI3 Serial Clock / GPIO 11
136	GPIO12	NAND_ALE/SPI3_CS1#	GPIO4_IO10	SPI3 Chip Select 0 / GPIO 12
105	GPIO13	GPIO1_IO01/OTG1_OC	GPIO1_IO01	SPI3 Chip Select 1 / GPIO 13
114	GPIO14	LCD_DATA00/PWM1_OUT	GPIO3_IO05	PWM / Clock / GPIO 14
115	GPIO15	LCD_DATA01/PWM2_OUT	GPIO3_IO06	PWM / Clock / GPIO 15
48	COMD TX	UART4_TX_DATA	GPIO1_IO28	COM D Transmit / GPIO
49	COMD RX	UART4_RX_DATA	GPIO1_IO29	COM D Receive / GPIO

2.5 Power Connections

The SoM-iMX6U requires a 3.3V supply for the Bus and I/O voltages. The 1.35V core voltage is regulated on module from the 3.3V. The on-processor RTC also requires 3.3V supplied by either a battery or the 3.3V power rail. The 5.0V USB VBUS voltage is regulated on module from 3.3V.

Table 17: Power Connections

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Description
3,4,141,142	3.3VCC	3.3VCC	3.3 Volt I/O voltage to the processor
1,2,52,53, 58,59,62,63,6 8,69,143, 144	GND	GND	Ground
119	VSTBY	3.3V_STBY	The SNVS regulator takes the SNVS_IN supply and generates the SNVS_CAP supply, which powers the real time clock and SNVS blocks
118	ALT_VCC	USB_OTGx_VBUS (Optional)	External VBUS Detection
101	AV_VCC	VDD_SNVS_IN (Optional)	Analog power. This is not required for the SoM-iMX6U
99	V_REF	ADC_VREFH (Optional)	ADC Voltage reference high

2.6 Boot Options

The SoM specification provides two pins for boot time configuration, BOOT_OPTION1 and BOOT_OPTION2. On the SoM-iMX6U, these are BMS1 and BMS2. The Boot Mode Select (BMS) pins allow the SoM-iMX6U to be low-level booted from either its internal ROM or USB.

The Module can high-level boot from either the Serial Flash or the eMMC (selected through the low-level boot loader). It is recommended to high-level boot from the Serial Flash.

Table 18: Boot Options

SODIMM Pin#	SoM Pin Name	Processor Pin Name(s)	Port Line	Description
41	BOOT_OPTION1	LCD_DATA05	GPIO3_IO10	Boot Mode Select 1
74	BOOT_OPTION2	LCD_DATA06	GPIO3_IO11	Boot Mode Select 2

2.7 Serial Data Flash

The Serial Data Flash is connected to SPI4 and uses the processors ENET2_RX_ER pin to enable it. The Serial Data Flash also has a Write Protect Provision. To Write Protect the Serial Data Flash pull SoM pin# 85 low. This pin is pulled up by a 10K ohm resistor on the module.

If this feature is required, it would be implemented on the carrier as a jumper or an I/O line.

2.8 Module Status LED

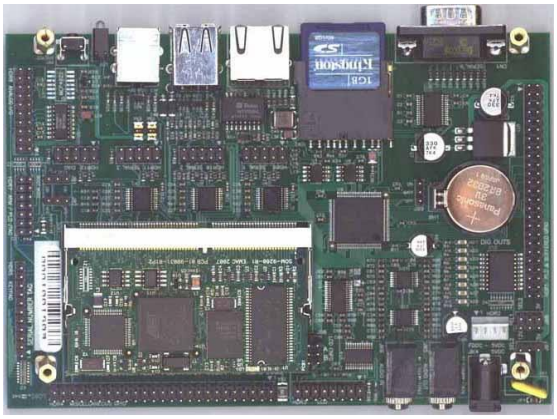
A green status LED (labeled LD1) is active-low and is controlled by port line NAND_DQS.

3 Design Considerations

One of the goals of the SoM-iMX6U is to provide a modular, flexible and inexpensive solution capable of delivering high-end microcontroller performance with low power requirements.

3.1 The EMAC SoM Carrier SoM-150ES

EMAC provides an off-the-shelf carrier for the SoM-iMX6U module, the SoM-150ES, which provides power to SoM modules and provides them with an extended range of I/O. This board comes with full schematics and BOM, and can be used as is, or as a reference for a customer's own design.



http://www.emacinc.com/products/system_on_module/SoM-150ES

EMAC also offers a semi-custom engineering service. By modifying an existing design, EMAC can offer quick-turn, low-cost engineering, for your specific application.

3.2 Power

The SoM-iMX6U requires a voltage of 3.3V at 300mA. For a bare-bones population, users can get away with using only 3.3V, and simply provide this to all the voltage inputs listed in Power Connections section.

3.2.1 Legacy

ALT_VCC is a legacy connection, required to support the SoM-400EM and may be used in future SoM modules. The SoM-iMX6U does not use this connection, so if general SoM compatibility is not an issue then this can be tied to 3.3V in a carrier designed for this SoM.

3.2.2 Battery Backup

The SoM-iMX6U real-time clock (RTC) requires a backup voltage to maintain its data. This backup voltage comes from the VSTBY pin, and should be connected to 3.3 volts.

The RTC will draw approximately 40uA when the processor is not powered by the 3.3V supply. When the module is powered no current is drawn from the backup battery supply. If the RTC is not needed, this can be tied to 3.3V.

The SoM-100ES and SoM-150ES provide battery backup voltage through a BR2032, which is a standard 3V 190mA/H 20MM coin battery that can be picked up from most electronics stores.

3.2.3 Analog Reference

No external Analog Reference voltage (VREF) is required for the SoM-iMX6U so this pin is normally a No Connect on the Module. An on-module 2.5V reference is provided. Analog input range is therefore 0 to 2.5V.

This Reference uses power and therefore can be turned off by setting LCD_DATA03 to a high, thus conserving about 2.2mA.

3.2.4 Analog Voltage

When designing power for the Analog subsystem there are two main considerations: range and accuracy.

- **Range**
  The AVCC normally will have an effect on the range, however, on the SoM-iMX6U this pin is a no-connect since the processor's Analog VCC (ADC_VREFH) is directly connected to a filtered 3.3V. This voltage reference defines the voltage range of the A/D convertor.

- **Accuracy**
  The accuracy of the A/D converters is determined by the voltage reference that is provided to the analog subsystem. Since the stability of the voltage between this reference and ground will affect the accuracy of the subsystem's measurements, this has been built into the SoM in this design. No external Analog Reference voltage is required for the SoM-iMX6U.

4 Software

The SoM-iMX6U offers a wide variety of software support from both open source and proprietary sources. The hardware core was designed to be software compatible with the NXP MCIMX6G1CVM05AA reference design, which is supported by Linux.

For more information on software support, please visit the EMAC Wiki Software Section at:

http://wiki.emacinc.com/wiki/product_wiki

4.1 Das U-Boot

EMAC utilizes Das U-Boot for its ARM based products. U-Boot is an open source/cross-architecture platform independent bootloader. It supports reading and writing to the flash, auto-booting, environmental variables, and TFTP. Das U-boot can be used to upload and run and/or reflash the OS or to run stand-alone programs without an OS. Products are shipped with a valid MAC address installed in flash in the protected U-boot environmental variable “ethaddr”. At boot time U-Boot automatically stores this address in a register within the MAC, which effectively provides it to any OS loaded after that point.

4.2 Embedded Linux

EMAC Open Embedded Linux is an open source Linux distribution for use in embedded systems. The EMAC OE Linux Build is based on the Open Embedded (www.openembedded.org) and Yocto (www.yoctoproject.org) Linux build system. Open Embedded is a superior Linux distribution for embedded systems. Custom Linux builds are also available on request.

The distribution contains everything a user could expect from a standard Linux kernel: powerful networking features, advanced file system support, security, debugging utilities, and countless other features.

The basic root file system includes:

- Busybox
- Hotplugging support
- APM utilities for power management
- Openssh SSH server
- lighttpd HTTP server
- JJFS2 or EXT4 file system with utilities

4.2.1 Linux with Xenomai Real Time Extensions

Xenomai provides real time extensions to the kernel and can be used to schedule tasks with hard deadlines and µs latencies. The Xenomai build is an additional module that can be added to the standard Linux kernel and is available for a one-time inexpensive support/installation fee.

http://www.xenomai.org/

4.2.2 Linux Packages

EMAC provides support for many Linux Packages such as: PHP, SQLite, Perl, SNMP, DHCP Server, etc. As with the Xenomai Package, other Packages can be added to the standard Linux file system and are available for a one-time inexpensive support/installation fee.

4.2.3 Linux Patches

In addition to standard Embedded Linux support, EMAC has released a number of patches and device drivers from the open source community and from internal EMAC engineering into its standard distribution. Along with kernel patches, EMAC provides the binaries for the kernel and root file system.

4.3 Qt Creator

Qt Creator is a cross-platform IDE (Integrated Development Environment) tailored to the needs of Qt developers but works well for Headless applications as well. EMAC provides sample code as projects that can be imported into Qt Creator. Qt Creator supports remote deployment and source debugging.

http://wiki.qt.io/Main

4.4 ARM EABI Cross Compiler

The popular open source gcc compiler has a stable build for the ARM family. EMAC uses the 4.9.1 version of the ARM EABI compiler. The Embedded Linux kernel and EMAC Qt Creator projects use this compiler for building ARM stand alone, and OS specific binaries. The EMAC Qt Creator provides source level debugging over Ethernet or serial using gdbserver. The Linux binaries for the ARM EABI cross compiler are available online along with the SDK. See the EMAC wiki for further information.