ADATA Technology Corp.

CompactFlash Memory Card

Datasheet

IPC39-XXXGX

4GB、8GB、16GB、32GB、64GB

Version 1

Document Number: R21-0269

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Key Features:

- **Capacity:** MLC 4GB~64GB
- **Form Factor:** CF 50 Pin Type 1
- **Compatibility:**
  - Complies CF Revision 6.0
  - S.M.A.R.T feature supported
  - NCQ Command supported
- **Performance**
  - Read: Up to 108MB/s
  - Write: Up to 47MB/s
- **Weight**
  - 12±1g
- **Power Consumption:**
  - Active: 2W-Max
  - Idle: 0.01W-Typical
- **Temperature:**
  - Operation:

    Commerical 0°C ~ 70°C

    Industrial -40°C ~ 85°C

    (8GB~32GB)
  - Non-operation: -50°C ~ 95°C
- **Humidity**
  - 0℃ to 55℃ / 5%~95% RH, non-condensing
- **Reliability**
  - MTBF: MLC 1,000,000 hours
  - Shock:1500G/0.5ms
  - Vibration:20G Peak, 10~2000Hz
- **Data Retention**
  - After all of the available P/E cycles are consumed, NAND cells on CF retain data for 12 months.

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Revision History

Version	Changes	Date	Editor
0	Preliminary	2014/4/17	Andy Lin
1	Modify Package Information	2014/6/24	Linda wu

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1.0 Product Description

1.1 Product Overview

The ADATA Compact Flash Card TM is an universal low cost data storage and communication media. It consists of a good compatible and high performance controller with advanced file management and wear-leverage technology to increase the transfer rate and life cycle of this solution. It also provides Error Correcting Code (ECC) function to detect and correct errors automatically. With In System Programming (ISP) function, it is very easy to load the up-to-date firmware and to solve most of the compatibility issue for new devices.

2.0 Features

- Targeted for portable and stationary applications
- Capacity：4GB, 8GB, 16GB, 32GB, 64GB
- Conforms to Compact Flash Card specification standard
- Fully compatible with PC Card ATA specification
- Support PIO 0~6 , MDMA 0~4 ,UDMA 0~7
- Support 72bit/1KB Error Correcting Code (ECC) function to detect and correct errors.
- Support In System Programming (ISP) function to load the firmware.
- Supports power down commands and sleep mode
- Support Wear Leverage function to maximize data endurance.
- +5 Volts or +3.3 Volts operation.
- Size：42.8×36.4×3.3 mm
- Durability : Minimum 10,000 insertion / removal cycles

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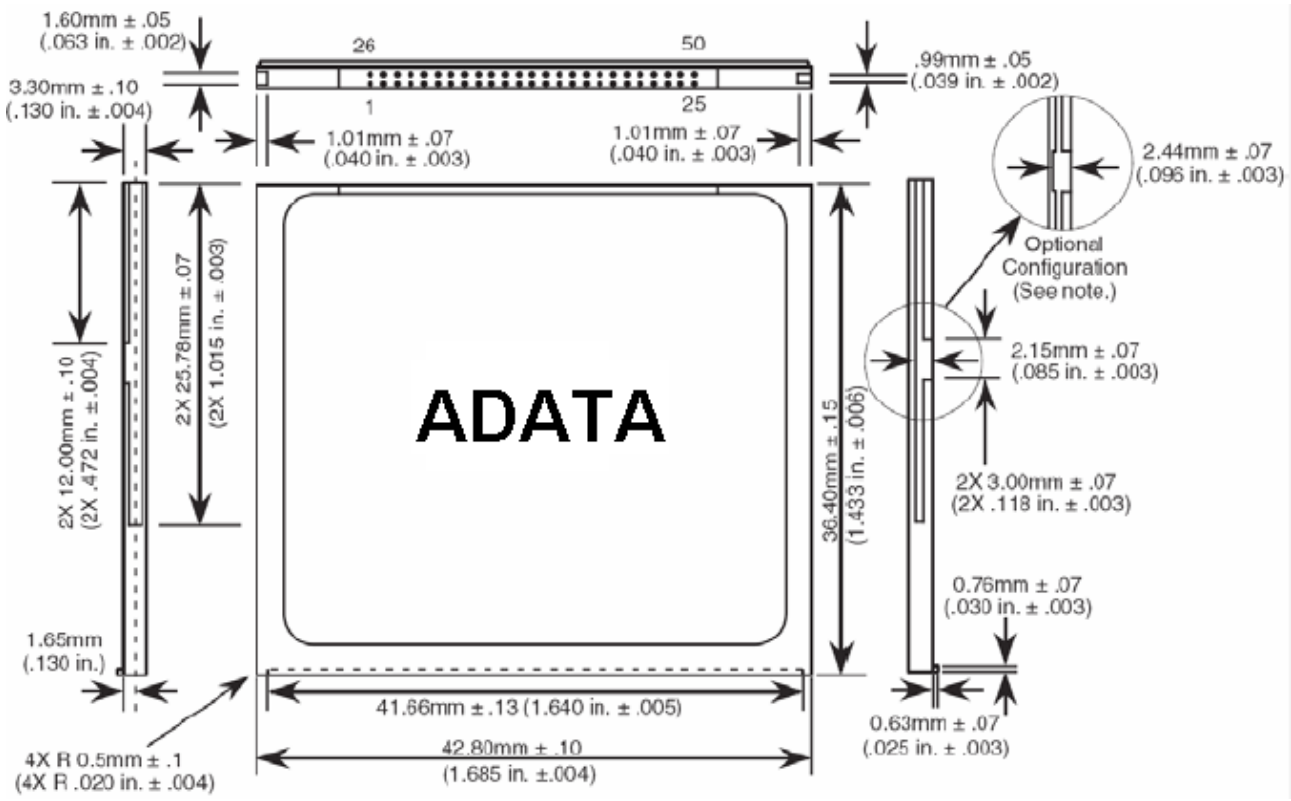
3.0 Mechanical Specification

3.1 Physical dimensions and Weight

Model	Height(mm)	Width(mm)	Length(mm)	Weight(gram)
4GB	Max 3.3	Max 36.4	Max 42.8	Max 12g
8GB	Max 3.3	Max 36.4	Max 42.8	Max 12g
16GB	Max 3.3	Max 36.4	Max 42.8	Max 12g
32GB	Max 3.3	Max 36.4	Max 42.8	Max 12g
64GB	Max 3.3	Max 36.4	Max 42.8	Max 12g

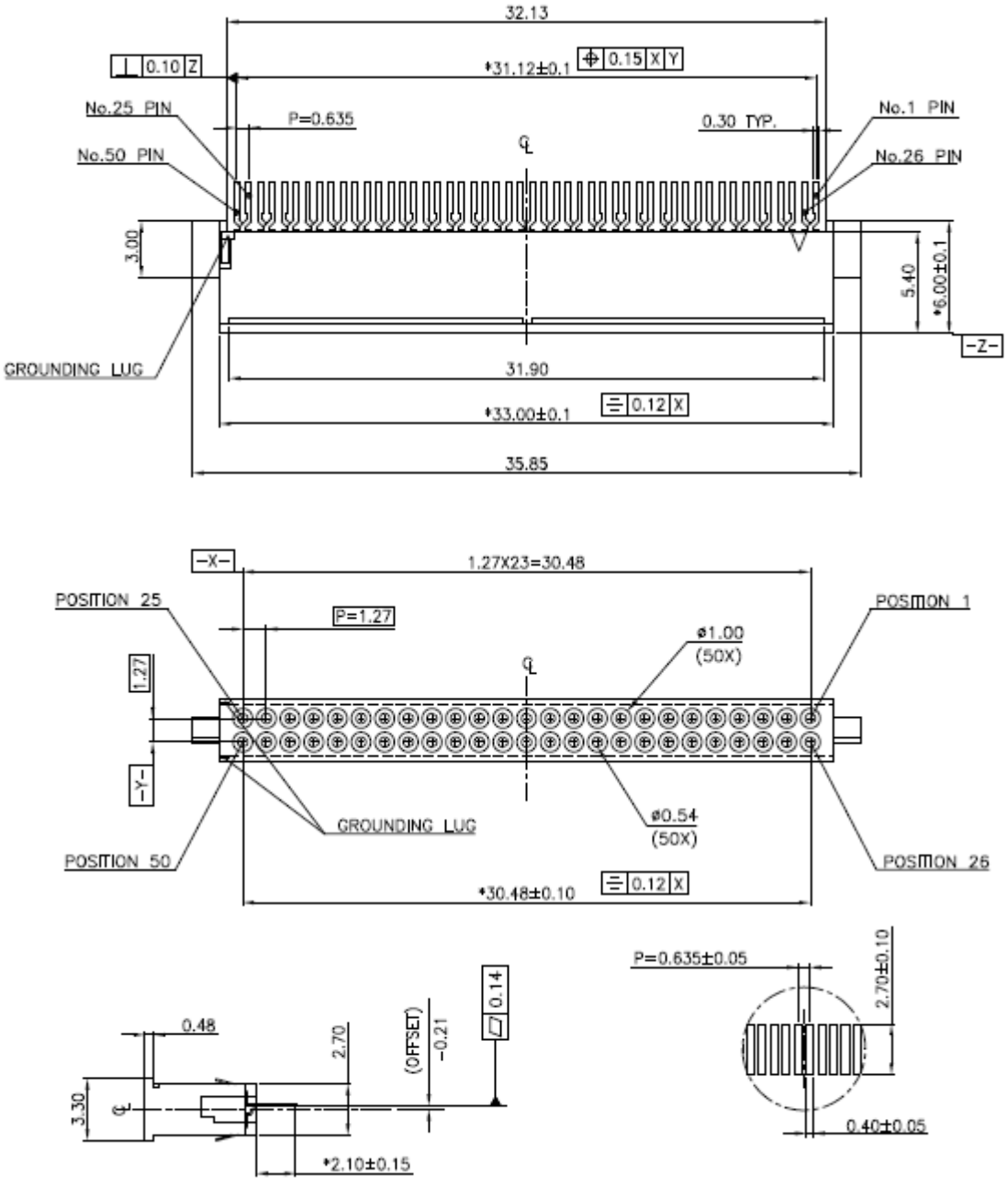


[Figure 3-1] Physical dimension

4.0 Electronic Specification

4.1 CompactFlash Memory Card Interface Connector

Drive Connector：CF-ATA type 50 pin



[Figure 4-1] CF-ATA Interface Connector

4.2 Pin Assignments and Pin Type

PC Card Memory Mode				PC Card I/O Mode				True IDE Mode[4]			
Pin Num	Signal Name	Pin Type	In, Out Type	Pin Num	Signal Name	Pin Type	In, Out Type	Pin Num	Signal Name	Pin Type	In, Out Type
1	GND		Ground	1	GND		Ground	1	GND		Ground
2	D03	I/O	I1Z, OZ3	2	D03	I/O	I1Z, OZ3	2	D03	I/O	I1Z, OZ3
3	D04	I/O	I1Z, OZ3	3	D04	I/O	I1Z, OZ3	3	D04	I/O	I1Z, OZ3
4	D05	I/O	I1Z, OZ3	4	D05	I/O	I1Z, OZ3	4	D05	I/O	I1Z, OZ3
5	D06	I/O	I1Z, OZ3	5	D06	I/O	I1Z, OZ3	5	D06	I/O	I1Z, OZ3
6	D07	I/O	I1Z, OZ3	6	D07	I/O	I1Z, OZ3	6	D07	I/O	I1Z, OZ3
7	-CE1	I	I3U	7	-CE1	I	I3U	7	-CS0	I	I3Z
8	A10	I	I1Z	8	A10	I	I1Z	8	A10[2]	I	I1Z
9	-OE	I	I3U	9	-OE	I	I3U	9	-ATA SEL	I	I3U
10	A09	I	I1Z	10	A09	I	I1Z	10	A09[2]	I	I1Z
11	A08	I	I1Z	11	A08	I	I1Z	11	A08[2]	I	I1Z
12	A07	I	I1Z	12	A07	I	I1Z	12	A07[2]	I	I1Z
13	VCC		Power	13	VCC		Power	13	VCC		Power
14	A06	I	I1Z	14	A06	I	I1Z	14	A06[2]	I	I1Z
15	A05	I	I1Z	15	A05	I	I1Z	15	A05[2]	I	I1Z
16	A04	I	I1Z	16	A04	I	I1Z	16	A04[2]	I	I1Z
17	A03	I	I1Z	17	A03	I	I1Z	17	A03[2]	I	I1Z
18	A02	I	I1Z	18	A02	I	I1Z	18	A02	I	I1Z
19	A01	I	I1Z	19	A01	I	I1Z	19	A01	I	I1Z
20	A00	I	I1Z	20	A00	I	I1Z	20	A00	I	I1Z
21	D00	I/O	I1Z, OZ3	21	D00	I/O	I1Z, OZ3	21	D00	I/O	I1Z, OZ3
22	D01	I/O	I1Z, OZ3	22	D01	I/O	I1Z, OZ3	22	D01	I/O	I1Z, OZ3
23	D02	I/O	I1Z, OZ3	23	D02	I/O	I1Z, OZ3	23	D02	I/O	I1Z, OZ3
24	WP	O	OT3	24	-IOIS16	O	OT3	24	-IOCS16	O	ON3
25	-CD2	O	Ground	25	-CD2	O	Ground	25	-CD2	O	Ground
26	-CD1	O	Ground	26	-CD1	O	Ground	26	-CD1	O	Ground
27	D11[1]	I/O	I1Z, OZ3	27	D11[1]	I/O	I1Z, OZ3	27	D11[1]	I/O	I1Z, OZ3
28	D12[1]	I/O	I1Z, OZ3	28	D12[1]	I/O	I1Z, OZ3	28	D12[1]	I/O	I1Z, OZ3
29	D13[1]	I/O	I1Z, OZ3	29	D13[1]	I/O	I1Z, OZ3	29	D13[1]	I/O	I1Z, OZ3
30	D14[1]	I/O	I1Z, OZ3	30	D14[1]	I/O	I1Z, OZ3	30	D14[1]	I/O	I1Z, OZ3
31	D15[1]	I/O	I1Z, OZ3	31	D15[1]	I/O	I1Z, OZ3	31	D15[1]	I/O	I1Z, OZ3
32	-CE2[1]	I	I3U	32	-CE2[1]	I	I3U	32	-CS1[1]	I	I3Z
33	-VS1	O	Ground	33	-VS1	O	Ground	33	-VS1	O	Ground
34	-IORD HSTROBE[10] HDMARDY[11]	I	I3U	34	-IORD HSTROBE[10] -HDMARDY[11]	I	I3U	34	-IORD[7] HSTROBE[8] -HDMARDY[9]	I	I3Z

PC Card Memory Mode				PC Card I/O Mode				True IDE Mode[4]			
Pin Num	Signal Name	Pin Type	In, Out Type	Pin Num	Signal Name	Pin Type	In, Out Type	Pin Num	Signal Name	Pin Type	In, Out Type
35	-IOWR	I	I3U	35	-IOWR	I	I3U	35	-IOWR[7]	I	I3Z
	STOP[10,11]				STOP[10,11]				STOP[8,9]		
36	-WE	I	I3U	36	-WE	I	I3U	36	-WE[3]	I	I3U
37	READY	O	OT1	37	-IREQ	O	OT1	37	INTRQ	O	OZ1
38	VCC		Power	38	VCC		Power	38	VCC		Power
39	-CSEL[5]	I	I2Z	39	-CSEL[5]	I	I2Z	39	-CSEL	I	I2U
40	-VS2	O	OPEN	40	-VS2	O	OPEN	40	-VS2	O	OPEN
41	RESET	I	I2Z	41	RESET	I	I2Z	41	-RESET	I	I2Z
42	-WAIT	O	OT1	42	-WAIT	O	OT1	42	IORDY[7]	O	ON1
	-DDMARDY[10]				-DDMARDY[10]				-DDMARDY[8]		OT1[13]
	DSTROBE[11]				DSTROBE[11]				DSTROBE[9]		
43	-INPACK	O	OT1	43	-INPACK	O	OT1	43	DMARQ	O	OZ1
	-DMARQ [12]				-DMARQ [12]						
44	-REG	I	I3U	44	-REG	I	I3U	44	-DMACK [6]	I	I3U
	-DMACK [12]				DMACK [12]						
45	BVD2	O	OT1	45	-SPKR	O	OT1	45	-DASP	I/O	I1U, ON1
46	BVD1	O	OT1	46	-STSCHG	O	OT1	46	-PDIAG	I/O	I1U, ON1
47	D08[1]	I/O	I1Z, OZ3	47	D08[1]	I/O	I1Z, OZ3	47	D08[1]	I/O	I1Z, OZ3
48	D09[1]	I/O	I1Z, OZ3	48	D09[1]	I/O	I1Z, OZ3	48	D09[1]	I/O	I1Z, OZ3
49	D10[1]	I/O	I1Z, OZ3	49	D10[1]	I/O	I1Z, OZ3	49	D10[1]	I/O	I1Z, OZ3
50	GND		Ground	50	GND		Ground	50	GND		Ground

[Table 4-1] Pin Assignments and Pin Type

Note: 1) These signals are required only for 16 bit accesses and not required when installed in 8 bit systems. Devices should allow for 3-state signals not to consume current.

2) The signal should be grounded by the host.

3) The signal should be tied to VCC by the host.

4) The mode is optional for CF+ Cards, but required for CompactFlash Storage Cards.

5) The -CSEL signal is ignored by the card in PC Card modes. However, because it is not pulled up on the card in these modes, it should not be left floating by the host in PC Card modes. In these modes, the pin should be connected by the host to PC Card A25 or grounded by the host.

6) If DMA operations are not used, the signal should be held high or tied to VCC by the host. For proper operation in older hosts: while DMA operations are not active, the card shall ignore this signal, including a floating condition

7) Signal usage in True IDE Mode except when Ultra DMA mode protocol is active.

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8) Signal usage in True IDE Mode when Ultra DMA mode protocol DMA Write is active.

9) Signal usage in True IDE Mode when Ultra DMA mode protocol DMA Read is active.

10) Signal usage in PC Card I/O and Memory Mode when Ultra DMA mode protocol DMA Write is active.

11) Signal usage in PC Card I/O and Memory Mode when Ultra DMA mode protocol DMA Read is active.

12) Signal usage in PC Card I/O and Memory Mode when Ultra DMA protocol is active.

13) Signal is a totem-pole output during Ultra DMA data bursts in True IDE mode.

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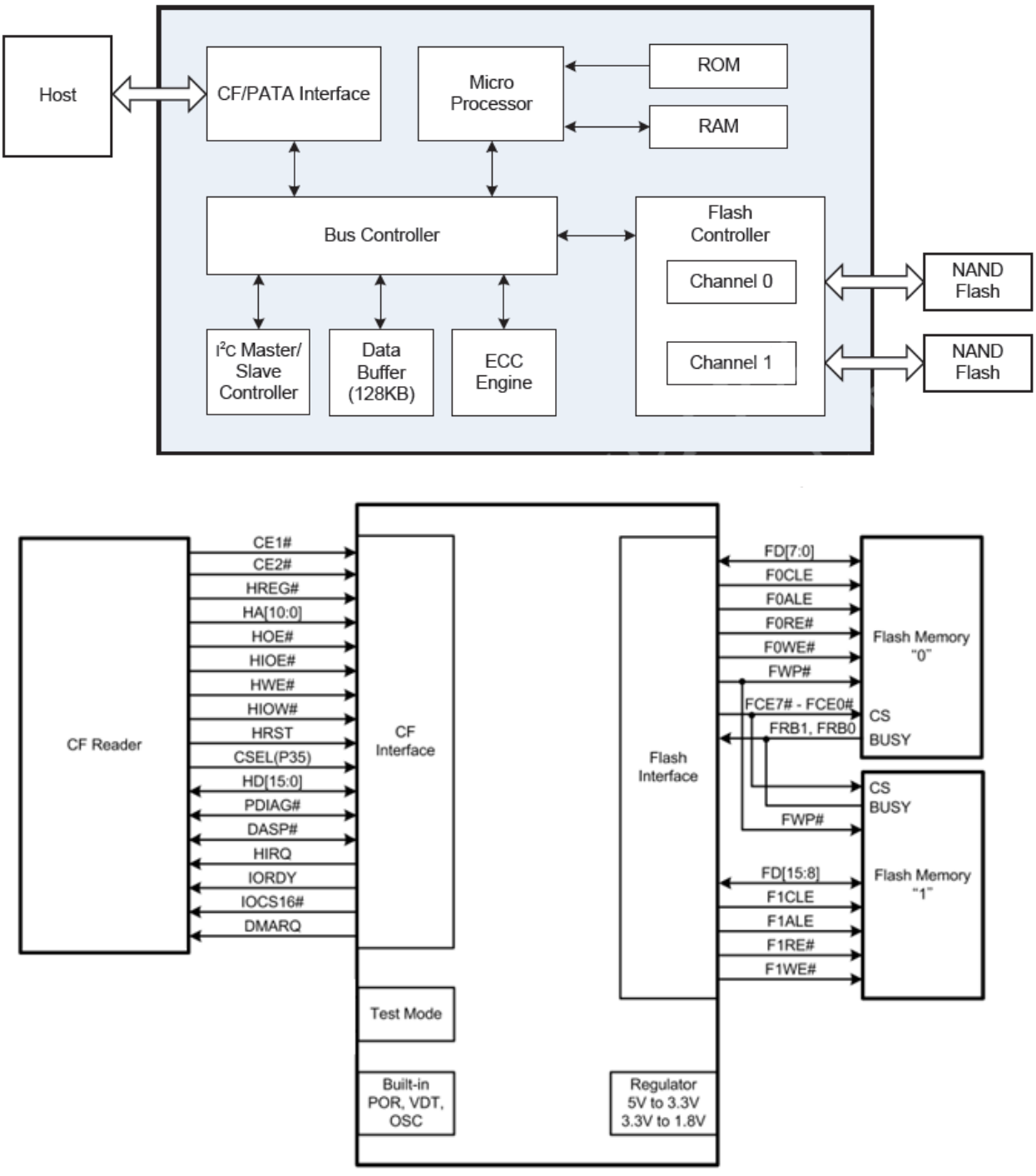
4.3 Function Block Diagram



[Figure 4-2] Function Diagram

4.4 ECC Descriptions

Using 72 bit BCH Error Correction Code with each channel, the ADATA CompactFlash memory card can correct up to 72 random bits in 1,204 bytes. The hardware executes parity generation and error detection/correction features.

4.5 SMART Command and Data Security

The ADATA CompactFlash Memory Card provides SMART command support that allows users to read spare and bad block information. Users can thus evaluate drive health at run time and receive an early warning before flash drive lifespan ends. The controller provides security commands for users to lock and unlock the drive by password or a hardware switch. The ADATA CompactFlash Memory Card also utilizes some customized commands to erase blocks for those users who require the highest level of security. Notably, ADATA can develop different security technologies when requested.

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4.6 Signal Description

Signal Name	Dir.	Pin	Description
A10 – A00 (PC Card Memory Mode)	I	8,10,11,12, 14,15,16,17, 18,19,20	These address lines along with the -REG signal are used to select the following: The I/O port address registers within the CompactFlash Storage Card or CF+ Card, the memory mapped port address registers within the CompactFlash Storage Card or CF+ Card, a byte in the card's information structure and its configuration control and status registers.
A10 – A00 (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
A02 - A00 (True IDE Mode)	I	18,19,20	In True IDE Mode, only A[02:00] are used to select the one of eight registers in the Task File, the remaining address lines should be grounded by the host.
BVD1 (PC Card Memory Mode)	I/O	46	This signal is asserted high, as BVD1 is not supported.
-STSCHG (PC Card I/O Mode) Status Changed			This signal is asserted low to alert the host to changes in the READY and Write Protect states, while the I/O interface is configured. Its use is controlled by the Card Config and Status Register.
-PDIAG (True IDE Mode)			In the True IDE Mode, this input / output is the Pass Diagnostic signal in the Master / Slave handshake protocol.
BVD2 (PC Card Memory Mode)	I/O	45	This signal is asserted high, as BVD2 is not supported.
-SPKR (PC Card I/O Mode)			This line is the Binary Audio output from the card. If the Card does not support the Binary Audio function, this line should be held negated.
-DASP (True IDE Mode)			In the True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
-CD1, -CD2 (PC Card Memory Mode)	O	26,25	These Card Detect pins are connected to ground on the CompactFlash Storage Card or CF+ Card. They are used by the host to determine that the CompactFlash Storage Card or CF+ Card is fully inserted into its socket.
-CD1, -CD2 (PC Card I/O Mode)			This signal is the same for all modes.
-CD1, -CD2 (True IDE Mode)			This signal is the same for all modes.
-CE1, -CE2 (PC Card Memory Mode) Card Enable	I	7,32	These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. -CE2 always accesses the odd byte of the word. -CE1 accesses the even byte or the Odd byte of the word depending on A0 and -CE2. A multiplexing scheme based on A0, -CE1, -CE2 allows 8 bit hosts to access all data on D0-D7. See Table 30, Table 33, Table 35, Table 39, Table 41 and Table 42. While (-) DMACK is asserted, -CE1 and -CE2 shall be held negated and the width of the transfers shall be 16 bits.
-CE1, -CE2 (PC Card I/O Mode) Card Enable			This signal is the same as the PC Card Memory Mode signal.
-CS0, -CS1 (True IDE Mode)			In the True IDE Mode, -CS0 is the address range select for the task file registers while -CS1 is used to select the Alternate Status Register and the Device Control Register. While –DMACK is asserted, -CS0 and –CS1 shall be held negated and the width of the transfers shall be 16 bits.

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Signal Name	Dir.	Pin	Description
-CSEL (PC Card Memory Mode)	I	39	This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host.
-CSEL (PC Card I/O Mode)			This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host.
-CSEL (True IDE Mode)			This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the True IDE Mode. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave.
D15 - D00 (PC Card Memory Mode)	I/O	31,30,29,28, 27,49,48,47, 6,5,4,3,2, 23, 22, 21	These lines carry the Data, Commands and Status information between the host and the controller. D00 is the LSB of the Even Byte of the Word. D08 is the LSB of the Odd Byte of the Word.
D15 - D00 (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
D15 - D00 (True IDE Mode)			In True IDE Mode, all Task File operations occur in byte mode on the low order bus D[7:0] while all data transfers are 16 bit using D[15:0].
GND (PC Card Memory Mode)	--	1,50	Ground.
GND (PC Card I/O Mode)			This signal is the same for all modes.
GND (True IDE Mode)			This signal is the same for all modes.

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Signal Name	Dir.	Pin	Description
-INPACK (PC Card Memory Mode except Ultra DMA Protocol Active)	O	43	This signal is not used in this mode.
-INPACK (PC Card I/O Mode except Ultra DMA Protocol Active) Input Acknowledge			The Input Acknowledge signal is asserted by the CompactFlash Storage Card or CF+ Card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the CompactFlash Storage Card or CF+ Card and the CPU. Hosts that support a single socket per interface logic, such as for Advanced Timing Modes and Ultra DMA operation may ignore the –INPACK signal from the device and manage their input buffers based solely on Card Enable signals.
-DMARQ (PC Card Memory Mode - Ultra DMA Protocol Active) -DMARQ (PC Card I/O Mode - Ultra DMA Protocol Active) DMARQ (True IDE Mode)			This signal is a DMA Request that is used for DMA data transfers between host and device. It shall be asserted by the device when it is ready to transfer data to or from the host. For Multiword DMA transfers, the direction of data transfer is controlled by -IORD and -IOWR. This signal is used in a handshake manner with (-)DMACK, i.e., the device shall wait until the host asserts (-)DMACK before negating (-)DMARQ, and re-asserting (-)DMARQ if there is more data to transfer. In PCMCIA I/O Mode, the -DMARQ shall be ignored by the host while the host is performing an I/O Read cycle to the device. The host shall not initiate an I/O Read cycle while -DMARQ is asserted by the device. In True IDE Mode, DMARQ shall not be driven when the device is not selected in the Drive-Head register. While a DMA operation is in progress, -CS0 (-CE1) and -CS1 (-CE2) shall be held negated and the width of the transfers shall be 16 bits. If there is no hardware support for True IDE DMA mode in the host, this output signal is not used and should not be connected at the host. In this case, the BIOS must report that DMA mode is not supported by the host so that device drivers will not attempt DMA mode operation. A host that does not support DMA mode and implements both PC Card and True IDE modes of operation need not alter the PC Card mode connections while in True IDE mode as long as this does not prevent proper operation in any mode.

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Signal Name	Dir.	Pin	Description
-IORD (PC Card Memory Mode except Ultra DMA Protocol Active)	I	34	This signal is not used in this mode.
-IORD (PC Card I/O Mode except Ultra DMA Protocol Active)			This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the CompactFlash Storage Card or CF+ Card when the card is configured to use the I/O interface.
-IORD (True IDE Mode – Except Ultra DMA Protocol Active)			In True IDE Mode, while Ultra DMA mode is not active, this signal has the same function as in PC Card I/O Mode.
-HDMARDY (All Modes - Ultra DMA Protocol DMA Read)			In all modes when Ultra DMA mode DMA Read is active, this signal is asserted by the host to indicate that the host is ready to receive Ultra DMA data-in bursts. The host may negate –HDMARDY to pause an Ultra DMA transfer.
HSTROBE (All Modes - Ultra DMA Protocol DMA Write)			In all modes when Ultra DMA mode DMA Write is active, this signal is the data out strobe generated by the host. Both the rising and falling edge of HSTROBE cause data to be latched by the device. The host may stop generating HSTROBE edges to pause an Ultra DMA data-out burst.
-IOWR (PC Card Memory Mode – Except Ultra DMA Protocol Active)	I	35	This signal is not used in this mode.
-IOWR (PC Card I/O Mode – Except Ultra DMA Protocol Active)			The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the CompactFlash Storage Card or CF+ Card controller registers when the CompactFlash Storage Card or CF+ Card is configured to use the I/O interface. The clocking shall occur on the negative to positive edge of the signal (trailing edge).
-IOWR (True IDE Mode – Except Ultra DMA Protocol Active)			In True IDE Mode, while Ultra DMA mode protocol is not active, this signal has the same function as in PC Card I/O Mode. When Ultra DMA mode protocol is supported, this signal must be negated before entering Ultra DMA mode protocol.
STOP (All Modes – Ultra DMA Protocol Active)			In All Modes, while Ultra DMA mode protocol is active, the assertion of this signal causes the termination of the Ultra DMA data burst.
-OE (PC Card Memory Mode)	I	9	This is an Output Enable strobe generated by the host interface. It is used to read data from the CompactFlash Storage Card or CF+ Card in Memory Mode and to read the CIS and configuration registers.
-OE (PC Card I/O Mode)			In PC Card I/O Mode, this signal is used to read the CIS and configuration registers.
-ATA SEL (True IDE Mode)			To enable True IDE Mode this input should be grounded by the host.

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Signal Name	Dir.	Pin	Description
READY (PC Card Memory Mode) -IREQ (PC Card I/O Mode) INTRQ (True IDE Mode)	O	37	In Memory Mode, this signal is set high when the CompactFlash Storage Card or CF+ Card is ready to accept a new data transfer operation and is held low when the card is busy. At power up and at Reset, the READY signal is held low (busy) until the CompactFlash Storage Card or CF+ Card has completed its power up or reset function. No access of any type should be made to the CompactFlash Storage Card or CF+ Card during this time. Note, however, that when a card is powered up and used with RESET continuously disconnected or asserted, the Reset function of the RESET pin is disabled. Consequently, the continuous assertion of RESET from the application of power shall not cause the READY signal to remain continuously in the busy state. I/O Operation – After the CompactFlash Storage Card or CF+ Card has been configured for I/O operation, this signal is used as -Interrupt Request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt. In True IDE Mode signal is the active high Interrupt Request to the host.
-REG (PC Card Memory Mode – Except Ultra DMA Protocol Active) Attribute Memory Select -REG (PC Card I/O Mode – Except Ultra DMA Protocol Active) -DMACK (PC Card Memory Mode when Ultra DMA Protocol Active) DMACK (PC Card I/O Mode when Ultra DMA Protocol Active) -DMACK (True IDE Mode)	I	44	This signal is used during Memory Cycles to distinguish between Common Memory and Register (Attribute) Memory accesses. High for Common Memory, Low for Attribute Memory. In PC Card Memory Mode, when Ultra DMA Protocol is supported by the host and the host has enabled Ultra DMA protocol on the card the, host shall keep the -REG signal negated during the execution of any DMA Command by the device. The signal shall also be active (low) during I/O Cycles when the I/O address is on the Bus. In PC Card I/O Mode, when Ultra DMA Protocol is supported by the host and the host has enabled Ultra DMA protocol on the card the, host shall keep the -REG signal asserted during the execution of any DMA Command by the device. This is a DMA Acknowledge signal that is asserted by the host in response to (-)DMARQ to initiate DMA transfers. In True IDE Mode, while DMA operations are not active, the card shall ignore the (-)DMACK signal, including a floating condition. If DMA operation is not supported by a True IDE Mode only host, this signal should be driven high or connected to VCC by the host. A host that does not support DMA mode and implements both PC Card and True-IDE modes of operation need not alter the PC Card mode connections while in True-IDE mode as long as this does not prevent proper operation all modes.
RESET (PC Card Memory Mode)	I	41	The CompactFlash Storage Card or CF+ Card is Reset when the RESET pin is high with the following important exception: The host may leave the RESET pin open or keep it continually high from the application of power without causing a continuous Reset of the card. Under either of these conditions, the card shall emerge from power-up having completed an initial Reset. The CompactFlash Storage Card or CF+ Card is also Reset when the Soft Reset bit in the Card Configuration Option Register is set.

Signal Name	Dir.	Pin	Description
RESET (PC Card I/O Mode) -RESET (True IDE Mode)			This signal is the same as the PC Card Memory Mode signal. In the True IDE Mode, this input pin is the active low hardware reset from the host.
VCC (PC Card Memory Mode) VCC (PC Card I/O Mode) VCC (True IDE Mode)	--	13,38	+5 V, +3.3 V power. This signal is the same for all modes. This signal is the same for all modes.
-VS1 -VS2 (PC Card Memory Mode) -VS1 -VS2 (PC Card I/O Mode) -VS1 -VS2 (True IDE Mode)	O	33 40	Voltage Sense Signals. -VS1 is grounded on the Card and sensed by the Host so that the CompactFlash Storage Card or CF+ Card CIS can be read at 3.3 volts and -VS2 is reserved by PCMCIA for a secondary voltage and is not connected on the Card. This signal is the same for all modes. This signal is the same for all modes.
-WAIT (PC Card Memory Mode – Except Ultra DMA Protocol Active) -WAIT (PC Card I/O Mode – Except Ultra DMA Protocol Active) IORDY (True IDE Mode – Except Ultra DMA Protocol Active) -DDMARDY (All Modes – Ultra DMA Write Protocol Active) DSTROBE (All Modes – Ultra DMA Read Protocol Active)	O	42	The -WAIT signal is driven low by the CompactFlash Storage Card or CF+ Card to signal the host to delay completion of a memory or I/O cycle that is in progress. This signal is the same as the PC Card Memory Mode signal. In True IDE Mode, except in Ultra DMA modes, this output signal may be used as IORDY. In all modes, when Ultra DMA mode DMA Write is active, this signal is asserted by the device during a data burst to indicate that the device is ready to receive Ultra DMA data out bursts. The device may negate -DDMARDY to pause an Ultra DMA transfer. In all modes, when Ultra DMA mode DMA Read is active, this signal is the data in strobe generated by the device. Both the rising and falling edge of DSTROBE cause data to be latched by the host. The device may stop generating DSTROBE edges to pause an Ultra DMA data in burst.
-WE (PC Card Memory Mode) -WE (PC Card I/O Mode) -WE (True IDE Mode)	I	36	This is a signal driven by the host and used for strobing memory write data to the registers of the CompactFlash Storage Card or CF+ Card when the card is configured in the memory interface mode. It is also used for writing the configuration registers. In PC Card I/O Mode, this signal is used for writing the configuration registers. In True IDE Mode, this input signal is not used and should be connected to VCC by the host.

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Signal Name	Dir.	Pin	Description
WP (PC Card Memory Mode) Write Protect	O	24	Memory Mode – The CompactFlash Storage Card or CF+ Card does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence.
-IOIS16 (PC Card I/O Mode)			I/O Operation – When the CompactFlash Storage Card or CF+ Card is configured for I/O Operation Pin 24 is used for the -I/O Selected is 16 Bit Port (-IOIS16) function. A Low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port.
-IOCS16 (True IDE Mode)			In True IDE Mode this output signal is asserted low when this device is expecting a word data transfer cycle.

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5.0 Product Specifications

5.1 System Interface and Configuration

- Supports CompactFlash card specification revision 6.0
- Supports PIO Modes 0, 1, 2, 3, 4, 5 and 6
- Supports Multi-Word DMA Modes 0, 1, 2, 3 and 4
- Supports Ultra DMA Modes 0, 1, 2, 3, 4, 5, 6 and 7
- Supports PCMCIA Extended Memory Mode
- Supports PCMCIA Ultra DMA Modes 0, 1, 2, 3, 4, 5, 6 and 7

5.2 System Performance

The ADATA CompactFlash Memory Card meets the performance requirements listed in below table.

The performance was measured on a computer system with following setup:

- Platform: ASUS P5K3 Deluxe (Intel P35 + ICH9)
- Operation Systems: Windows XP SP3
- Testing Utility: CrystalDiskMark v3.0

IPC39	Windows OS	
	IDE Mode	
	IDE Mode Read	IDE Mode Write
4GB	37MB/s	12MB/s
8GB	68MB/s	13MB/s
16GB	101MB/s	24MB/s
32GB	108MB/s	47MB/s

Actual performance may vary depending on use conditions and environment

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5.3 Drive Capacity

Capacity	Capacity	Cylinders	Heads	Sectors	Max LBA
4GB	3.74GB	7,785	16	63	7,847,280
8GB	7.47GB	15,538	16	63	15,662,304
16GB	14.92GB	31,045	16	63	31,293,360
32GB	29.82GB	62,041	16	63	62,537,328
64GB	59.63GB	16,383	15	63	125,059,072

5.4 Supply Voltage

Item	Requirements
Allowable voltage	3.3V ± 5% or 5V ± 10%
Allowable noise/ripple	100mV p-p or less

5.5 System Power Consumption

Power	Typical
Active	< 2 W
Idel/Standby/Sleep	< 0.01W

5.6 System Reliability

MTBF	1,000,000 Hours

5.7 Environmental Specifications

Feature	Operating	Non-Operating
Temperature	0 to 70°C / -40 to 85°C	-50°C to 95°C
Humidity	0℃ to 55℃ / 5%~95% RH, non-condensing	
Vibration	20G Peak, 10~2000Hz	
Shock	1500G, duration 0.5ms, Half Sine Wave	

*Note: Depends on Flash memory specifications.

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5.8 Parameter Setting

Item	Parameter Setting
Vender Name	ADATA
Product Name	ICF CARD
Model Name	ADATA IPC39-XXXGM
CF Card Mode	PIO Mode：6 UDMA(IDE)：7 CF Mode：Removable IDE Mode：Fixed

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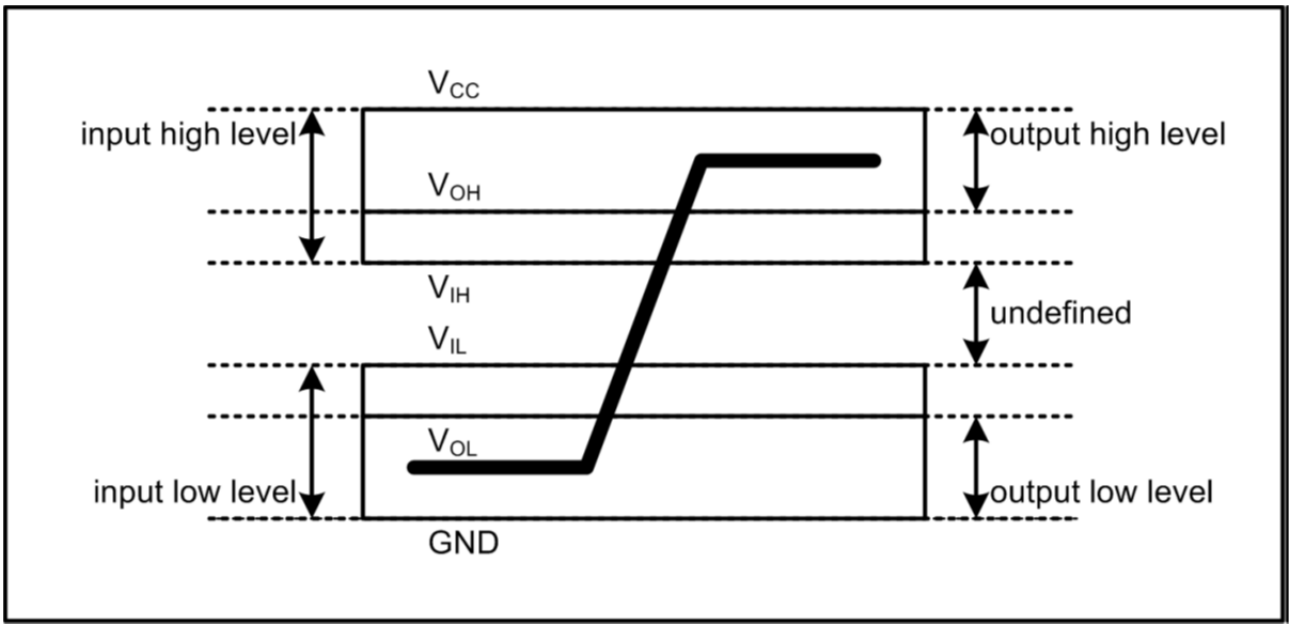
6.0 AC/DC Characteristics

6.1 General DC Characteristics

6.1.1 Definitions of VIH, VCC, VOH, VOL



[Figure 6-1-1] Definitions of VIH, VCC, VOH, VOL

6.1.2 DC Characteristics for Host Interface (VCC = 5V / 3.3V)

Parameter	Symbol	Min	Max	Unit	Remark
Supply Voltage 5V (from Host)	V_{CC}	4.5	5.5	V	
Supply Voltage 3.3V(from Host)	V_{CC}	2.97	3.63	V	
High Level Output Voltage	V_{OH}	2.5		V	
Low Level Output Voltage	V_{OL}		0.4	V	
High Level Input Voltage	V_{IH}	2.4		V	Non-schmitt trigger
		2.05		V	Schmitt trigger[1]
Low Level Input Voltage	V_{IL}		0.6	V	Non-schmitt trigger
			1.25	V	Schmitt trigger[1]
Pull-Up Resistance	R_{PU}	52.7	141	kΩ	
Pull-Down Resistance	R_{PD}	47.5	172	kΩ	

[Table 6-1-2] CompactFlash Interface at 5.0V / 3.3V

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6.1.3 DC Characteristics of 3.3V I/O Pins (other than Host Interface)

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Supply Voltage (V_{IO})	VCC3H	2.7	3.3	3.6	V	
	VCC3F	2.6	3.3	3.6	V	
High Level Output Voltage	V_{OH}	0.9 x V_{IO}			V	
Low Level Output Voltage	V_{OL}			0.1 x V_{IO}	V	
High Level Input Voltage	V_{IH}	1.51	1.62	1.75	V	Non-schmitt trigger
		1.61	1.72	1.84	V	Schmitt trigger[2]
Low Level Input Voltage	V_{IL}	1.51	1.62	1.74	V	Non-schmitt trigger
		1.38	1.49	1.61	V	Schmitt trigger[2]
Pull-Up Resistance	R_{PU}	20	70	120	kΩ	
Pull-Down Resistance	R_{PD}	20	70	120	kΩ	

[Table 6-1-3] CompactFlash Interface I/O at 3.3V

6.1.4 DC Characteristics of 1.8V I/O Pins (other than Host Interface)

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Supply Voltage (V_{IO})	VCC3F	1.7	1.8	1.95	V	
High Level Output Voltage	V_{OH}	0.9 x V_{IO}			V	
Low Level Output Voltage	V_{OL}			0.1 x V_{IO}	V	
High Level Input Voltage	V_{IH}	0.8	0.89	1.0	V	Non-schmitt trigger
		0.88	1.0	1.12	V	Schmitt trigger[2]
Low Level Input Voltage	V_{IL}	0.8	0.89	1.0	V	Non-schmitt trigger
		0.59	0.74	0.89	V	Schmitt trigger[2]
Pull-Up Resistance	R_{PU}	45	150	255	kΩ	
Pull-Down Resistance	R_{PD}	45	150	255	kΩ	

[Table 6-1-4] CompactFlash Interface I/O at 1.8V

Note:

1. Include CE1#, CE2#, HREG#, HOE#, HIOE#, HWE#, HIOW# pins.
2. Include RST#, T0, T1, T2 pins.

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6.2 Internal IP Characteristics

6.2.1 Power On Reset

Parameter		Min	Max	Unit
Detect Voltage			1.3	V
Operating Voltage Range		0	1.65	V
Delay Time	Rise		4.5	μs
	Fall		2	μs

[Table 6-2-1] Power On Reset

6.2.2 Oscillator

Parameter	Min	Max	Unit
Power Down Current		0	μA
Frequency Stability	15	26	MHz

[Table 6-2-2] Oscillator

6.2.3 2.7V Voltage Detector

Parameter		Min	Max	Unit
Detect Voltage Range	VRR	1.4	2.9	V
	VFR	1.3	2.8	V
Delay Time	Rise		4.5	μs
	Fall		1.5	μs

Parameter		Min	Max	Unit
Detect Voltage Range	VRR		4.0	V
	VFR		3.9	V
Delay Time	Rise		4.5	μs
	Fall		1.5	μs

Table [6-2-3] Voltage Detector

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6.2.4 Series Termination Required for Ultra DMA Operation

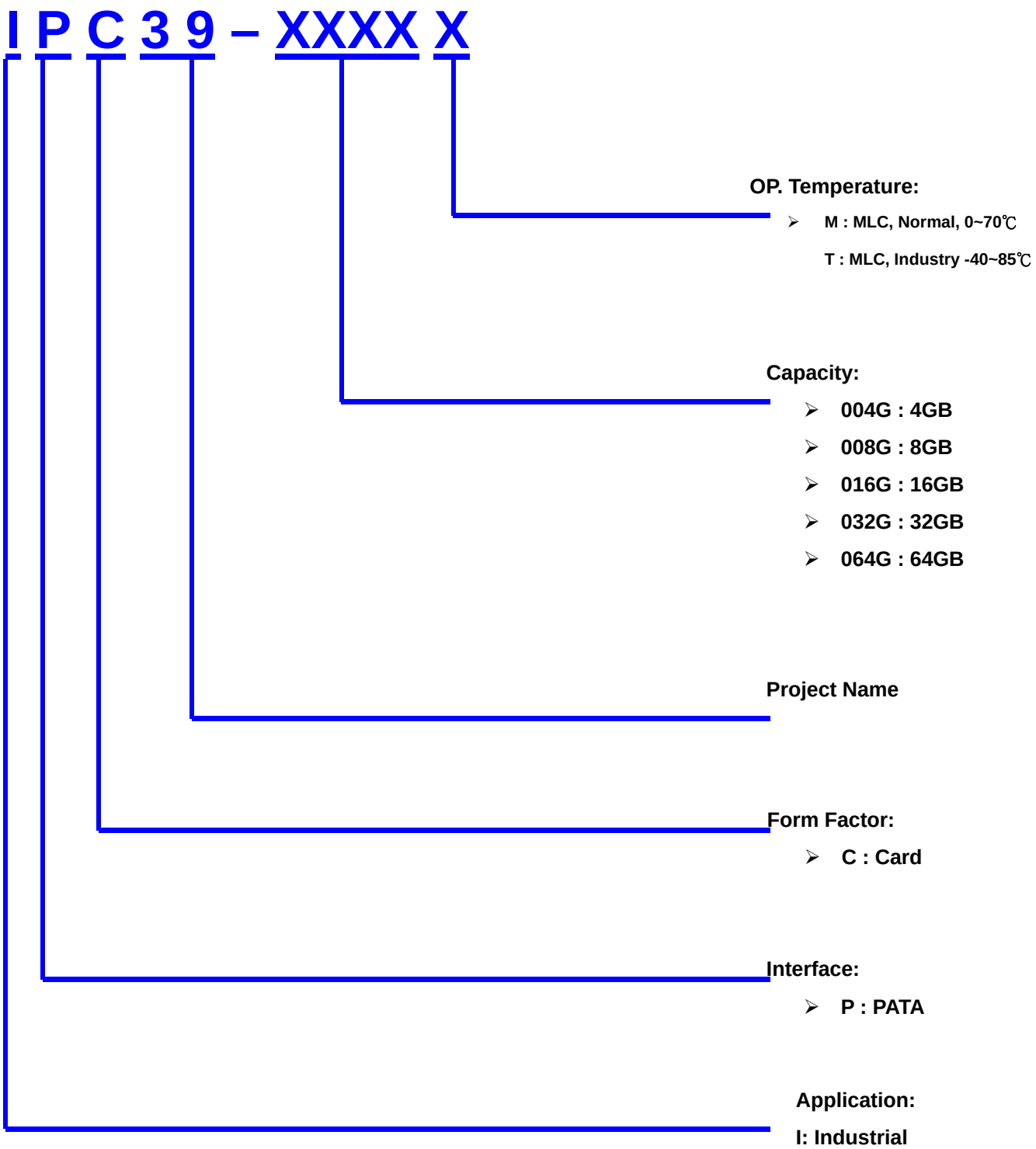
Series termination resistors are required at both the host and the card for operation in any of the Ultra DMA modes. Table 15 describes typical values for series termination at the host and the device

Signal	Host Termination	Device Termination
-IORD (-HDMARDY, HSTROBE)	22 ohm	82 ohm
-IOWR (STOP)	22 ohm	82 ohm
-CS0, -CS1	33 ohm	82 ohm
A00, A01, A02	33 ohm	82 ohm
-DMACK	22 ohm	82 ohm
D15 through D00	33 ohm	33 ohm
DMARQ	82 ohm	22 ohm
INTRQ	82 ohm	22 ohm
IORDY (-DDMARDY, DSTROBE)	82 ohm	22 ohm
-RESET	33 ohm	82 ohm
NOTE – Only those signals requiring termination are listed in this table. If a signal is not listed, series termination is not required for operation in an Ultra DMA mode. Figure 24 shows signals also requiring a pull-up or pull-down resistor at the host. The actual termination values should be selected to compensate for transceiver and trace impedance to match the characteristic cable impedance.		

[Table 6-2-4] Typical Series Termination for Ultra DMA

7.0 Ordering Information

7.1 Model Name



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7.1 Packing

CF card front side label working instruction

Front side label for CF Card

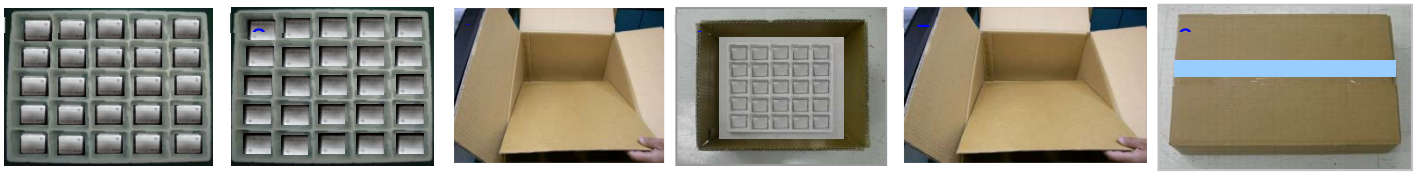
IPC39(M)	IPC39(T)
	

Back side label for CF Card

CF Card on back label rule :

a:CF woluld be pasted 35*30mm lable on the back side(showed as picture),please see lable principle for detail information.

Bulk Packing: Put CF on tray in 0.5 Cuft^3 paper box. Standard packing with 250pcs per box.



A. Put 25pcs CF card on each white tray. Put the back side of CF up, and the arrangement should be identical.
B. Cross-stack trays while second layer being put on lower layer.(refer pic2)
C. Total 250pcs per box with ten trays and a empty tray on the top.
D. Use plastic film to fasten all trays to avoid shaking.
E. Use 0.5 Cuft^3 paper box, and firstly put one pad on the bottom of box. (refer pic3)
F. Put well-wraped trays on the box. Standard packing 250pcs per box(10*25pcs as pic4) If being not full of one box, please fill in with stuff.
G. Finally, put a pad on top in the box. (refer pic5)
H. Use gummed tape to seal the box. (refer pic6)

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Attachment

Printing Coding Rule

Model	Capacity	B.(PN)	C.(PID)	D.(SN)
IPC39(M)	4GB	IPC39-004GM	As SA	As Below
	8GB	IPC39-008GM		
	16GB	IPC39-016GM		
	32GB	IPC39-032GM		
	64GB	IPC39-064GM		

Label (Sample)

Definition for internal and external S/N

EX: 1E1520000001 (Total 12 codes)

Code	1	2	3-4	5	6-12
Definition	Factory.	Year	Week	Type	Counting No.
Example	1	E	15	2	0000001

Explanation:

1.) Code 1: ADATA Production Factory.

2.) Code 2: Produced year, 2010=A, 2011=B……

3.) Code 3-4: Produced week

4.) Code 5: Package type

5.) Code 6-12: Serial No. by decimal counting method. Total 7 numbers. And, it will begin from 0000001 per each new WIP.

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