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SoM-5282EM
Users Manual

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SoM-5282EM Users Manual rev1.2

Table of Contents

1. Introduction

This document describes EMAC's SoM-5282EM (SBC) module. The SoM-5282EM is a system on module, designed to be backwards compatible with EMAC's SoM-400EM, but taking advantage of the more powerful MCF5282 processor.

Like the SoM-400EM, the SoM-5282EM has an onboard PHY, 3 serial ports, a RTC, a programmable clock synthesizer, onboard flash and RAM.

In addition to these standard SoM features, the SoM-5282EM also features a much faster 32-bit core, open source software support, and a wide range of controller IO pins.

1.1. Features

- **Small, SoM compatible SODIMM form factor 2.66" x 1.50"**
- **10/100 Base-T Ethernet with on-board PHY**
- **RTC**
- **8/16M DRAM**
- **2/4M Flash**
- **PLL synthesized clocks, 14.3MHz, 8MHz, 200KHz**
- **Strong open source support including Das U-Boot and μClinux**
- **Standard core M5282EVB architecture compatible with most commercial software packages**
- **Freescale MCF5282 Coldfire core with:**
  - **64MHz 32-bit RISC core**
  - **2K instruction and data cache**
  - **DRAM controller**
  - **BDM**
  - **Queued SPI Port**
  - **3 Serial Ports with handshake lines**
  - **8 channels of 10-bit A/D**
  - **General Purpose Timers with external interface for Counters/PWM**
  - **JTAG**
  - **2.0 CAN**

2. **Hardware**

2.1. Specifications

- **VOLTAGE REQUIREMENTS:** 3.3V (and 5V for 5V analog if required)
- **CURRENT REQUIREMENTS:** 500 mA max.
- **OPERATING TEMPERATURE:** 0 - 70 degrees Centigrade, humidity range without condensation 0% to 90% RH.
- **DIMENSIONS:** SODIMM form factor with dimensions of 2.66" x 1.50".
- **PROCESSOR:** Freescale MCF5282 microcontroller
- **DRAM:** 8 or 6M of fast DRAM
- **FLASH:** 2 or 4M flash
- **RTC**
- **I/O:** 144 pin SODIMM connection providing
  - **External Bus Interface**: 22 address x 16 data
  - **BDM**: standard background debug module
  - **Ethernet:** onboard PHY provides 10/100 base-T Ethernet signals.
  - **QSPI**: queued SPI port with 3 multiplex-able chip selects
  - **Serial Ports**: 3 serial ports or 14 pins of GPIO
  - **A/D:** 8 multiplex-able AtoD inputs or 8 GPIO
  - **External IRQs:** 6 external IRQs or 6 GPIO
  - **Timer/Counters:** 4 input capture/output compare timer pins with sync pin or 5 GPIO
  - **JTAG**: bit banged JTAG out, or 4 additional general-purpose timer pins.
  - **CAN**: 2.0 CAN interface or 2 GPIO
  - **CLOCKS**: PLL synthesized 8M, 200K, 14.3M clock outputs

2.2. Real Time Clock

The SoM-5282EM provides a DS1305 real time clock/calendar on board the module. Battery backup is provided by the carrier board through the VSTBY pin.

2.3. External Connections

The SoM-5282 connects to a carrier board containing its connectors, power supply and any expansion IO, through a standard gold-plated SODIMM 144 pin connection (top half shown below).

The SoM model will fit in any standard SODIMM socket. These connections are designed to be compatible with all EMAC SoM products.

The remainder of this section describes the pinout as it applies specifically to the SoM-5282EM processor.

2.3.1. External Bus

The SoM-5282EM provides a flexible external bus for connecting peripherals. The CPLD of the SoM-100ES connects through a subset of these connections.

SODIMM Pin#	Pin Name	Processor Pin	Description
100	GP_CS1	~CS1~/PJ1	General purpose Chip select 1 from the processor or GPIO
98	GP_CS2	~CS2~/PJ2	General purpose Chip select 2 from the processor or GPIO
108	GP_CS3	~CS3~/PJ3	General purpose Chip select 3 from the processor or GPIO
16	~OE	~OE~/PE7	Output enable, asserts when an external device can drive the data bus or GPIO
83	~WR	R/~W~/PE4	Indicates the direction of the bus transfer or GPIO
6	~RST_IN	~RSTIN	Reset input to the processor.
43	~RST_OUT	~RSTOUT	Reset output from the processor
44	~EA	~TEA~/PE5	Error condition on a bus transfer or GPIO
85	~RD/TIP	NC	Not connected on the SoM-5282EM
72	ALE/~TS	~TS~/PE1/SYNCA	Transfer-Start Asserted at the start of a transfer to indicate a valid address or GPIO
26,35,33,31,28,109,111,113,10,12,18,14,37,5,11,9,7,13,97,17,15,104	Address bus A0-A21	Address bus A0-A21	Address lines from the processor. These same lines are tied to the internal memory of the SoM-100ES, so must always be used as address lines (not GPIO)
29,27,25,22,23,21,19,20,8,24,34,70,77,81,84,86	Data Bus D0-D15	Data Bus D16-D31	High data lines from the processor, these are used for word access to peripherals as per the design recommendations. Again, like the data lines, these pins must be used as data pins only as they are attached to the memory of the module.

2.3.2. BDM – Module specific interface

The SoM-5282EM brings out the full BDM connection of the processor. These pins are routed on the SoM-100ES to a P&E wiggler compatible header, which can be used for full, low level source debugging through either a proprietary package such as Metroworks Codewarrior, or an open source program such as gdb, which fully supports source level debugging of the processor. This can even be used to step though the low level internals of the Linux kernel itself.

On the SoM-5282EM, these pins come out the pins that have been delegated “module specific” in the SoM specification.

SODIMM Pin#	Pin Name	Processor Pin	Description
45	MS0	~BKPT~/TMS	Hardware breakpoint assertion
46	MS1	~TA~/PE6	External data transfer complete or GPIO
47	MS2	DSCLK/~TRST	Serial interface to debug module
48	MS3	DSI/TDI	Bit communication for module commands
49	MS4	DSO/TDO	Bit communication for command responses
50	MS5	NC	Reset input to the processor.
51	MS6	NC	Reset output from the processor
57,56,55,54	MS10-7	DDATA0-3	Display captured process data
60	MS11	TCLK	JTAG test logic clock
61	MS12	CLOCKOUT	Reflects the system clock
64,65,66,67	MS13-16	PST0-3	Indicates core status

2.3.3. JTAG/GPTB

The SoM specifications for the JTAG header are filled by GPIO/TimerB pins on the SoM-5282. These connections will allow CPLD/FPGAs to be programmed in circuit via a program running from the processor.

Alternatively these pins can be used as GPT pins, which can be used as counters or PWM.

SODIMM Pin#	Pin Name	Processor Pin	Description
139	JTAG_TCK	GPTB0/PTB0	JTAG clock -> port B0
137	JTAG_TDI	GPTB1/PTB1	JTAG serial in -> port B1
138	JTAG_TDO	GPTB2/PTB2	JTAG serial out ->port B2
140	JTAG_TMS	GPTB3/PTB3	JTAG operation mode ->port B3

2.3.4. One-Wire

The SoM specification calls for a one-wire port. On the SoM-5282EM this is just connected to GPIO pin of the processor for bit-banged operation.

SODIMM Pin#	Pin Name	Processor Pin	Description
116	LOCAL1W	SIZ0/PE2/ SYNCB	Maxim One-Wire network signal/GPIO. Connected directly to PE2 of the processor. This configuration will not be capable of driving standard One-Wire networks, or OW devices expecting power from the pin. Users with demanding one-wire applications are referred to the SoM-400EM or the SoM-NE64EM.

2.3.5. Ethernet

The SoM-5282EM provides a LX972 Ethernet phy IC on board. Carrier designers need only run these lines through the appropriate magnetics layer to have a functional Ethernet connection.

The LED/configuration pins state at reset determines the Ethernet's configuration (10-baseT, 100-base-T,autoconfig) and the function of the LED's. The SoM-100ESR3 pulls them all high, which configures the chip for network autoconfig, with LED1 functioning as active low link, and LED3 functioning as active low Rx status.

SODIMM Pin#	Pin Name	LXT972 Pin	Description
88	LED_TX/ CFG_0	LED_TX/ CFG_0	Ethernet LED/Configuration pin
89	LED_LINK/ CFG_1	LED_LINK/ CFG_1	Ethernet LED/Configuration pin
90	LED_RX/ CFG_2	LED_RX/ CFG_2	Ethernet LED/Configuration pin
94	Ethernet_Rx-	Ethernet_Rx-	Low differential Ethernet receive line
92	Ethernet_Rx+	Ethernet_Rx+	High differential Ethernet receive line
93	Ethernet_Tx-	Ethernet_Tx-	Low differential Ethernet transmit line
91	Ethernet_Tx+	Ethernet_Tx+	High differential Ethernet transmit line

2.3.6. QSPI

The Coldfire processor provides a queued SPI module for communicating with peripheral devices. This bus is connected internally to the RTC, which uses SPI_CS3 (not brought out to the card fingers). Linux users can use the open source mcf_qspi driver provided by EMAC, or the earlier 2.4 driver available in the main μClinux tree.

SODIMM Pin#	Pin Name	Processor Pin	Description
122	SPI_MI	QSPI_DIN/PQS1	QSPI serial data in
121	SPI_MO	QSPI_DOUT/PQS0	QSPI serial data out
120	SPI__SCK	QSPI_CLK/PQS2	QSPI serial clock out
123	SPI_CS0	QSPI_CS0/PQS3	QSPI slave select line 3
124	SPI_CS1	QSPI_CS1/PQS4	QSPI slave select line 4
110	SPI_CS2*	QSPI_CS2/PQS5	QSPI slave select line 5

2.3.7. Serial Ports

The SoM-5282 provides 3 serial ports. Typically the SoM specification calls for Com0 to be the terminal port, which is the default for both Maxims Tini OS, and μClinux. However, com0 on the 5282 processor provides handshaking pins, which go to waste on a terminal port. Therefore the SoM-5282EM design swaps Com1 and Com3. A patch is provided for Linux 2.4 and Linux 2.6 to swap them back in the OS.

SODIMM Pin#	Pin Name	Processor Pin	Description
71	COM1_RXD	SDA/PAS1/ URXD2	COM1 receive/GPIO
73	COM1_TXD	SCL/PAS0/ UTXD2	COM1 transmit/GPIO
38	COM2_RXD	URXD1/PUA3	COM2 receive/GPIO
36	COM2_TXD	UTXD1/PUA2	COM2 transmit/GPIO
82	COM2_RTS/GPIO	DTOUT1/PTD2/~URTS1-0	COM2 RTS/GPIO
78	COM2_CTS/GPIO	DTOUT0/PTD0/~UCTS1-0	COM2 CTS/GPIO
103	COM3_RXD_	URXD0/PUA1	COM3 receive/GPIO
102	COM3_TXD	UTXD0/PUA0	COM3 receive/GPIO
107	COM3_DSR/GPIO	DTIN0/PTD1/ ~UCTS1-0	COM3 DSR /GPIO
106	COM3_DTR/GPIO	DTIN1/PTD3/ ~URTS1-0	COM3 DTR/GPIO
76	COM3_RI/GPIO	DTIN2/PTC1/ ~UCTS1-0	COM3 RING/GPIO
30	COM3_DCD/GPIO	DTIN3/PTC3/ ~URTS1-0	COM3 DCD/GPIO
39	COM3_RTS/GPIO	DTOUT3/PTC2/~URTS1-0	COM3 RTS/GPIO
79	COM3_CTS/GPIO	DTOUT2/PTC0/~UCTS1-0	COM3 CTS/GPIO

2.3.8. GPIO

This section provides for the SoM general purpose IO section. With the exception of the clocks, all of these pins can be configured to be general-purpose digital ports. They can also be configured to take advantage of several of the functions of the 5282's internal silicon. All of the internal A/D ports are brought out here, as well as all of the available IRQs and the pins for general-purpose timer A.

A/D:
The Analog to digital pins can handle 8 channels directly, or can multiplex up to 18 inputs. It can handle 10bit resolution and 7us conversion, with the enhanced multiply and accumulate unit behind it, this can make quite a capable signal processor.

Timer/Counters:
General-purpose timer modules on the Coldfire are 16-bit timers; with independently programmable input-capture or output compare lines. These can be used for a wide variety of timed applications, including counters and PWM.

For more information on the AtoD and Timer functions of the MCF5282 processor, users are referred to the *MCF5282 ColdFire Microcontroller User's Manual* .

SODIMM Pin#	Pin Name	Processor Pin	Description
75	IRQ1/GPIO	~IRQ1~/PNQ1	edge port IRQ 1/GPIO
32	IRQ3/GPIO	~IRQ3~/PNQ3	edge port IRQ 3/GPIO
40	GPIO0/IRQ4*	~IRQ4~/PNQ4	edge port IRQ 4/GPIO0
42	GPIO1/IRQ5*	~IRQ5~/PNQ5	edge port IRQ 5/GPIO1
87	GPIO2/IRQ6*	~IRQ6~/PNQ6	edge port IRQ 6/GPIO2
80	GPIO3/IRQ7*	~IRQ7~/PNQ7	edge port IRQ7/GPIO3
125	GPIO4	GPTA0/PTA0	Timer A GPT0 signal or GPIO4
126	GPIO5	GPTA1/PTA1	Timer A GPT1 signal or GPIO5
127	GPIO6	GPTA2/PTA2	Timer A GPT2 signal or GPIO6
128	GPIO7	GPTA3/PTA3	Timer A GPT3 signal or GPIO7
129	GPIO8	AN0/PQB0/ANW	Queued AtoD0/GPIO8
130	GPIO9	AN1/PQB1/ANX	Queued AtoD1/GPIO9
131	GPIO10	AN2/PQB2/ANY	Queued AtoD2/GPIO10
132	GPIO11	AN3/PQB3/ANZ	Queued AtoD3/GPIO11
133	GPIO12	AN52/PQA0/MA0	Queued AtoD4/GPIO12/ Analog multiplexer control low
134	GPIO13	AN53/PQA1/MA1	Queued AtoD5/GPIO13 Analog multiplexer control high
135	GPIO14	AN55/PQA3/ETRIG1	Queued AtoD6/GPIO14/External Analog Queue trigger
136	GPIO15	AN56/PQA4/ETRIG2	Queued AtoD7/GPIO15/External Analog Queue trigger
105	~LDAC/~GPIO	SIZ1/PE3/SYNCA	LDAC control for external DtoA converter or GPIO or timer A external sync
114	8MHz	8MHz	General purpose 8MHz clock
115	200KHz	200KHz	General purpose 200KHz clock
117	14.3MHz	14.3MHz	General purpose 14.3MHz clock

2.3.9. CAN

The 5282 processor provides a full 2.0 queued CAN bus implementation. Note: check the 5282 errata sheets for potential problems when using the CAN bus.

SODIMM Pin#	Pin Name	Processor Pin	Description
96	P5.0/CAN_TX	CANTX/PAS2/UTXD2	CAN transmit
95	P5.1/CAN_RX	CANRX/PAS3/URXD2	CAN receive

2.4. Power

The SoM-5282EM requires a 3.3V rail to supply core voltage to the processor. It also provides several other voltage inputs which can be used to enable and change the characteristics of different parts of the module (NVRAM, 5V analog, filtered analog referenced). If these functions are not required their power pins can just be tied to 3.3V.

SODIMM Pin#	Pin Name	Processor pin-SoM connection	Description
3,4,141,142	3.3VCC	3.3VCC	3.3 Volt voltage core to the processor
1,2,52,53, 58,59,62,63 ,68,69,143, 144	GND	GND	Ground
119	VSTBY	VSTBY-RTC bat backup	Voltage standby, this is the backup voltage provided to the internal RAM of the processor, as well as to the voltage backup of the RTC. If non-volatile RAM, RTC readings are not important for the application, this can be attached to the 3.3V rail.
118	VPULLUP	NA-RTC power	This is a 5V input to the SoM, provided here for backwards compatibility. If the application in question is 5282 specific, it can be connected to 3.3V(the RTC can accept a 3.3V power supply)
101	VDDA/VDDH	VDDA/VDDH	Analog power. This voltage provides power to the internal analog circuitry of the 5282 processor. It can run anywhere from the 3.3V rail to the 6V. This voltage will determine the maximum value of the reference voltage, and will be the voltage driven out when the pins are used as outputs. Note: During power up VDDA/VDDH should never trail the 3.3V power signal by more then .3 volts. This can lead to an internal latch up of the processor.
99	VRH	VRH	Analog Reference voltage. This is the reference signal the Analog inputs use to represent the maximum voltage for digital conversion. This input cannot be higher than VDDA/VDDH.

2.5. Boot Options

The SoM specification provides two pins for boot time configuration. On the SoM-5282EM, these are JTAG_EN and PTA0. JTAG_EN is a hardware configuration pin, that enables JTAG functionality over the BDM pins. PTA0 is the same pin as GPIO pin 4, and is brought out here as well for hardware compatibility. It has no hardware configuration function, and user could use software to code a boot option. This may be changed in a future revision to an RCON function.

SODIMM Pin#	Pin Name	Processor Pin	Description
41	BOOT_OPTION1	JTAG_EN	Enable JTAG over the BDM pins
74	BOOT_OPTION2	GPTA0/PTA0	User Defined/GPIO

3. Design Considerations

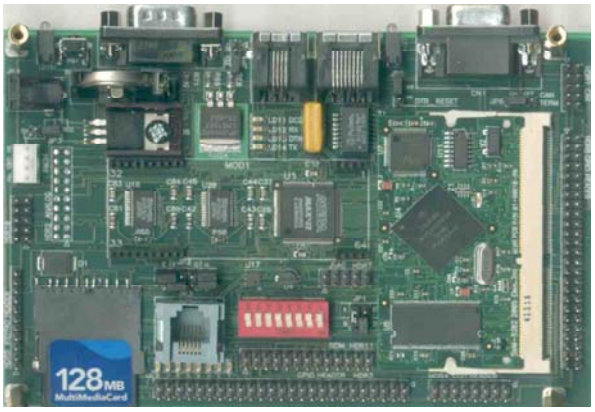
One of the goals of the SoM-5282EM is to provide a modular, flexible and inexpensive solution capable of delivering high-end microcontroller performance.

3.1. The EMAC SoM Carrier-SoM-100ES

EMAC provides an off the shelf carrier for it's SoM modules, the SoM-100ES, which provides power to SoM modules and provides them with an extended range of I/O. This board comes with full schematics and BOM, and can be used as is, or as a reference for a customers own design.

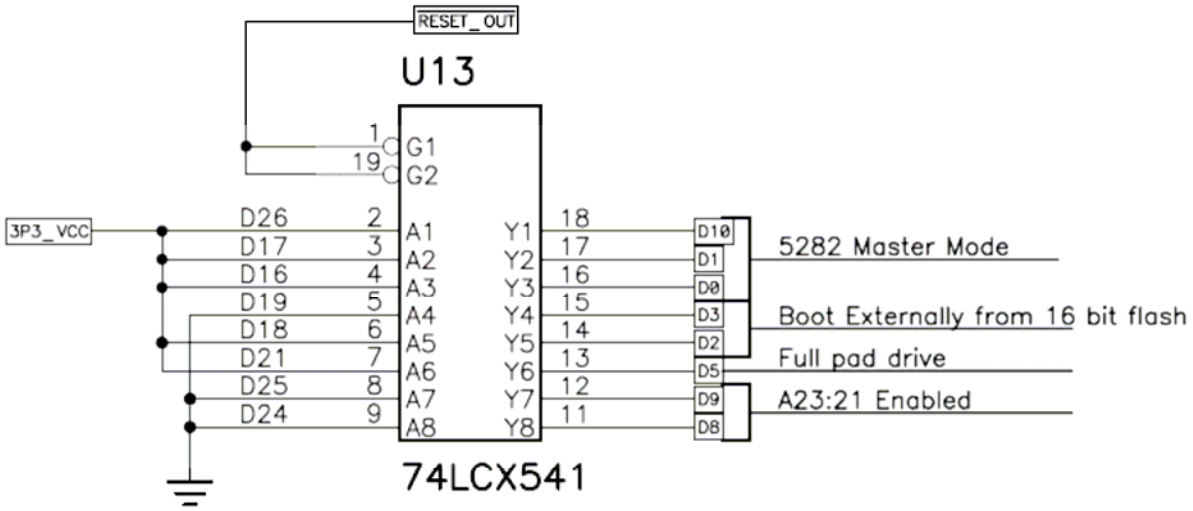
http://www.emacinc.com/som/som100es.htm

EMAC also offers a semi-custom engineering service. By modifying an existing design, EMAC can offer a quick turn, low cost engineering, for your specific application.



3.2. Configuration

At reset, the SoM-5282R0's processor requires its default configuration to be latched onto its data lines at reset. A diagram from the SoM-100ES schematic is shown below, showing a popular valid configuration used in most 5282 products. For further details about Coldfire processor configuration, see the *MCF5282 ColdFire Microcontroller User's Manual* section 27, the CCM. Also refer to the carrier board schematic.



3.3. Power

The SoM-5282EM is requires a core voltage of 3.3V and 500mA For a bare-bones population, users can get away with using only 3.3V, and simply provide this to all the voltage inputs listed in 2.3.10. This, however will provide only a subset of the 5282's full capability.

3.3.1. Legacy

VPULLUP is a legacy connection, required to support the SoM-400EM and may be used in future SoM modules. If general SoM compatibility is not an issue then this can be tied to 3.3V.

3.3.2. Battery Backup

The SoM-5282EM contains 3 potentially non-volatile memory areas, the flash, the real time clock, and the internal RAM of the processor. The flash is always non-volatile, but the internal RAM and real time clock require a backup voltage to maintain their data. This backup voltage comes from the VSTBY pin, it should be between 1.8 and 3.6 volts, and be capable of providing a instantaneous surge of 7 mA.

The battery backed RAM will draw 20 μA while no power is supplied to the board, and the RTC will draw 400 nA. Since the RAM's current draw is so much higher than the RTC, the SoM-5282 provides a zero-ohm resistor in series with the RAMs VSTBY, which can be removed from the module if it's not needed. If the RTC and the NVRAM are not needed, this can just be tied to 3.3V.

The SoM-100ES provides battery backup voltage through a socketable BR2032, which is a standard 3V 190mA/H 20MM coin battery that can be picked up from most electronics stores.

3.3.3. Analog Voltage

When designing power for the Analog subsystem there are 4 major considerations, range and accuracy output drive, and rise time.

- **Range**
  The VDDA/VDDH pins provide the range. These pins provide power to the analog subsystem, and can take any voltage from 3.3 to 6Volts. The power supplied to the analog subsystem limits the range of voltages that can be accurately measured. The internal analog converters cannot measure a voltage higher than their power rail.

- **Accuracy**
  The accuracy of the A/D converters is determined by the VRH pin, which provides the reference voltage to the analog subsystem. The stability of the voltage between this pin and ground will effect the accuracy of the subsystem's measurements. For many cases a filter cap is sufficient, since these are only 10 bit converters, however in some environments more robust filters may need to be employed. The VRH pin cannot be at a higher voltage than VDDA/VDDH.

- **Drive**
  Another consideration when designing the Analog power supply is the output drive. The A/D conversion pins are also configurable as outputs. In this mode the output voltage will drive to the voltage supplied on VDDA/VDDH. The SoM-100ES provides 5.6 volts to VDDA/VDDH through a diode drop from a charge pump to the 5V rail, and provides the reference voltage through a standard ref-02 IC.

- **Rise Time**
  The final consideration for Analog power design is the rise time. MCF5282 processors run the risk of locking up if their core 3.3 voltage gets further than .3 volts ahead of VDDA/VDDH during power up. Therefore if separate supplies are used some sort of sequencing must be considered. The SoM-100ES drains its 3.3V rail through a power diode to the 5.6 volt rail, which forces the analog subsystem to follow the main rail closely enough to avoid any potential lockups.

If users don't need highly accurate readings, and are ok with a 3 volt limitation on the analog readings, then both VRH and VDDA/VDDH can be tied to 3.3V. For a more in-depth description of Analog power design users are referred to section 28 of the *MCF5282 ColdFire Microcontroller User's Manual.*

4. Software

The SoM-5282EM offers a wide variety of software support from both open source and proprietary sources. The hardware core was designed to be software compatible with the Motorola M5282EVB reference design, which is supported in most Coldfire SDK's.

4.1. Eclipse

EMAC provides sample code and drivers for the SoM-5282EM as CDT projects within the free Eclipse IDE. Eclipse is a powerful open-source Java based IDE. It has plug-ins for Java and C, development and debugging, as well as several other languages.

http://www.eclipse.org/

EMAC offers a free download of Eclipse 3.0, complete with JDK 1.4.2, the Eclipse CDT plug-in, and the pre-integrated Tini distribution. We also offer the CTD projects standalone, for easy integration with Eclipse for Linux and Mac users.

ftp://SoM:sompublic@ftp.emacinc.com/index.html

4.1.1. Eclipse CDT plug-in

The Eclipse CDT plug-in provides a powerful graphical IDE for C development. This plug-in relies on GNU Make to build its files, so its projects are highly portable to other IDE's (or lack of them completely). It also offers a MI based debugger, for plugging into the newer gdbs.

http://www.eclipse.org/cdt/

4.2. Das U-Boot

The SoM-5282EM is distributed with Das U-Boot installed. U-Boot is an open source/cross-architecture platform independent bootloader. It supports reading and writing to the flash, auto-booting, environmental variables, and tftp. Das U-boot can be used to upload and run and/or reflash the OS on the SoM-5282EM without the use of a BDM cable, or to run stand-alone programs without an OS. SoM-5282EM modules are shipped with a valid MAC address installed in flash in the protected ethaddr environmental variable of U-Boot. At boot time U-Boot automatically stores this address in the register of the FEC, which effectively provides it to any OS loaded after that point.

The official Das U-Boot project does not currently fully support the 5282 processor, but a full and open source patched version is available through EMAC. This version contains work by EMAC, and several open source developers and will be released into the main distribution as soon as it is approved.

This version supports both internal and external boot, and can see the full flash of the 2M or 4M populations. By default SoM-5282EM's are shipped with the bootloader in both internal and external flash.
http://sourceforge.net/projects/u-boot

4.3. μClinux

μClinux is an open source Linux distribution for use with MMU-less systems such as the Coldfire processor. It's a full distribution; build around either a patched 2.4 kernel, or the new 2.6 kernel, which fully supports the embedded m68k architecture. EMAC will support newer kernel version in the future once they become stable.

The distribution contains everything a user could expect from a standard Linux kernel, powerful networking features, advanced file system support, security, gdbserver for source debugging over ethernet, etc…

The SoM-5282EM will work out of the box with the standard μClinux distribution, and EMAC provides the most up to date distribution via ftp. The SoM-5282EM comes preinstalled with a 2.6 build as of the date of this manual.

www.uclinux.org

4.3.1. μClinux with RTAI

EMAC also maintains the open source port RTAI to the μClinux 2.4 5282 kernel. RTAI provides real time extensions to the kernel and can be used to schedule tasks with hard deadlines and μs latencies. In the future EMAC will be supporting RTAI on the 2.6 kernel.

www.rtai.org

4.3.2. μClinux 2.6 drivers

In addition to standard μClinux support, EMAC has released the a number of patches and device drivers from the open source community and from internal EMAC engineering into it's standard distribution. Pending approval from the main tree, these changes will eventually be moved into the main distribution, but are pre-released as stable builds supporting EMAC hardware. All open source 5282 software is stored in the EMAC public CVS, accessable at

server: mail.emacinc.com
repository: opt.public

login: coldfirertai
passwd: 5282-rtai

Alternatively, SoM software can be obtained from EMAC SoM ftp site.
Access to the site can be obtained by request by emailing coldfirertai@emacinc.com .

EMAC μClinux drivers are maintained within the EMAC μClinux distribution, and as stand-alone Eclipse CDT builds. At the time of this documents writing, the following new drivers/patches were available:

- **EMAC build integration**

The EMAC SoM-5282EM vendor option, and new drivers have been added to the μClinux build tree, and show up in the high-level configuration menus. Default configuration, device creation, and scripts have been added to vendors/EMAC/SOM5282EM/

- **Serial port swap**

EMAC provides a patch to swap serial ports ttyS0 and ttyS2 in software. This reflects the hardware of the SoM-5282, which brings Com1 out it's Com3 port and vice-versa. This is done to enable the use of hardware handshake lines on the third com port.

- **Enabled Cache**

The current 2.6 kernel disables the Cache of the 5282 by default. This is because originally the Cache of the 5282 was broken. Freescale has since fixed this, however, and all SoM-5282EM's ship with fully functional caches. This patch enables the cache in software, greatly increasing the throughput of the processor.

- **QSPI**

The MCF5282 queued SPI driver has been ported and moved into the 2.6 kernel. Also, it's low level calls have be broken out to allow module stacking, which is currently used by the real time clock driver, and will be used by the new SoM-100ES drivers that are currently in development. For details on it's API users are referred to the README within it's project. A test application, loopback.c, is provided in the project which can be used to test the driver and demonstrates how to use it's character driver interface.

- **DS1305RTC**

The SoM-5282EM has a built in Dallas real time clock, the DS1305. The DS1305RTC driver stacks on top of the QSPI driver and provides standard real time clock ioctl's for setting and reading the date of the DS1305. Real time clock nodes (/dev/rtc, major 10, minor 135) will hook this driver, so it can be used by the hwclock and date programs(included in the standard distribution) .

- **General Purpose IO**

A driver for controlling the 32 digital ports of the SoM-100ESR2 is available. This driver can bit configure the ports bitwise as input, output, read the current state, and set latch pins configured to be outputs.

- **Character LCD**

A character LCD driver is available providing the API of the sourceforge lcd-mod project. The provides support for character LCD's based on the HD44780 controller at various row/column configurations. It accepts input as a formatted string that can be passed in through standard POSIX read/write calls, or by piping input directly from the command line.

- **MMC**

A driver for accessing the MMC socket of the SoM-100ESR2 over the qspi layer is available. This driver stacks on top of the QSPI driver and provides a standard 2.6 block interface to the card, which can then be formatted, mounted, etc…

- **FEC patch**

A small patch was made to the FEC (fast Ethernet controller)driver to prevent it from disabling the second serial port on initialization. This has already been moved into the main CVS but is not yet available in the standard μClinux stable distribution.

4.4. M68k-Elf-Tools

The popular open source gcc compiler has a stable build for the m68k family. Which can be used for building Coldfire applications using the –m5307 flag. The Das U-boot project, μClinux, EMAC Eclipse CDT projects and Codewarrior IDE's all use this compiler for building Coldfire stand alone, and OS specific binaries. Open source patched versions of gdb are available for source level debugging over either the BDM port or over the Ethernet using gdbserver.

http://gcc.gnu.org/

Pre-built binaries by the μClinux community are available here:

http://www.uclinux.org/pub/uClinux/m68k-elf-tools/

4.5. Commercial Solutions

In addition to the open source community, a wide variety of commercial software development solutions are available as well. The most popular probably being Metrowerks CodeWarrior for the Coldfire processor family.

http://www.metrowerks.com/MW/Develop/Embedded/ColdFire/Default.htm

Other solutions include the 5282LITE SDK with embedded stack from Viola Systems, Quadros RTXC, Micro Digital SMX, as well as a host of others.

4.6. Java

EMAC plans to support Java on the SoM-5282 in the future probably through the use of Waba or SuperWaba. This will allow users of the TINI based SoM-400EM an upgrade path to faster processor.

Appendix A – Pin-out by number

The following table compares the pinout of the SoM-400EM, the SoM-5282EM, and the SoM-100ES carrier by pin number.
Customers can also obtain an xls spreadsheet of the pins for easy CAD importation and sorting from the SoM ftp site upon purchase of any SoM product.

PIN	DS400 Pin	Coldfire Pin	Module Pin
1	GND	GND	GND
2	GND	GND	GND
3	3.3VCC	3.3VCC	3.3VCC
4	3.3VCC	3.3VCC	3.3VCC
5	A13	A13/PG5	A13
6	~RST_IN	~RSTIN	~RST_IN
7	A16	A16/PF0	A16
8	NC	D24/PA0	D8*
9	A15	A15/PG7	A15
10	A8	A8/PG0	A8
11	A14	A14/PG6	A14
12	A9	A9/PG1	A9
13	A17	A17/PF1	A17
14	A11	A11/PG3	A11
15	A20	A20/PF4	A20

16	~PSEN	~OE~/PE7	~OE
17	A19	A19/PF3	A19
18	A10	A10/PG2	A10
19	D6	D22/PB6	D6
20	D7	D23/PB7	D7
21	D5	D21/PB5	D5
22	D3	D19/PB3	D3
23	D4	D20/PB4	D4
24	NC	D25/PA1	D9*
25	D2	D18/PB2	D2
26	A0	A0/PH0	A0
27	D1	D17/PB1	D1
28	A4	A4/PH4	A4
29	D0	D16/PB0	D0
30	P1.4/INT2	DTIN3/PTC3/~URTS1-0	COM3_DCD/GPIO
31	A3	A3/PH3	A3
32	P1.5/~INT3	~IRQ3~/PNQ3	IRQ3/GPIO
33	A2	A2/PH2	A2
34	NC	D26/PA2	D10*
35	A1	A1/PH1	A1
36	P1.3/TXD1	UTXD1/PUA2	COM2_TXD
37	A12	A12/PG4	A12
38	P1.2/RXD1	URXD1/PUA3	COM2_RXD
39	P1.6/INT4	DTOUT3/PTC2/~URTS1-0	COM3_RTS/GPIO
40	P1.1/T2EX	~IRQ4~/PNQ4	GPIO0/IRQ4*
41	P1.7/~INT5	JTAG_EN	BOOT_OPTION1
42	P1.0/T2OUT	~IRQ5~/PNQ5	GPIO1/IRQ5*
43	~RST_OUT	~RSTOUT	~RST_OUT
44	~EA	~TEA~/PE5	~EA
45	CRS	~BKPT~/TMS	MS0
46	TXEN	~TA~/PE6	MS1
47	COL	DSCLK/~TRST	MS2
48	RXERR	DSI/TDI	MS3
49	RXDV	DSO/TDO	MS4
50	MDC	NC	MS5
51	MDIO	NC	MS6
52	GND	GND	GND
53	GND	GND	GND
54	TXD3	DDATA3/PDD7	MS7
55	TXD2	DDATA2/PDD6	MS8
56	TXD1	DDATA1/PDD5	MS9
57	TXD0	DDATA0/PDD4	MS10
58	GND	GND	GND
59	GND	GND	GND
60	TXCLK	TCLK	MS11
61	RXCLK	CLKOUT	MS12
62	GND	GND	GND
63	GND	GND	GND
64	RXD0	PST0/PDD0	MS13
65	RXD1	PST1/PDD1	MS14

66	RXD2	PST2/PDD2	MS15
67	RXD3	PST3/PDD3	MS16
68	GND	GND	GND
69	GND	GND	GND
70	NC	D27/PA3	D11*
71	P3.0/RXD0	SDA/PAS1/URXD2	COM1_RXD
72	ALE	~TS~/PE1/SYNCA	ALE/~TS
73	P3.1/TXD0	SCL/PAS0/UTXD2	COM1_TXD
74	P5.3	GPTA0/PTA0	BOOT_OPTION2
75	P3.2/~INT0	~IRQ1~/PNQ1	IRQ1/GPIO
76	P5.5/~PCE1	DTIN2/PTC1/~UCTS1-0	COM3_RI/GPIO
77	NC	D28/PA4	D12*
78	P5.7/~PCE3	DTOUT0/PTD0/~UCTS1-0	COM2_CTS/GPIO
79	P3.3/~INT1	DTOUT2/PTC0/~UCTS1-0	COM3_CTS/GPIO
80	P5.4/~PCE0	~IRQ7~/PNQ7	GPIO3/IRQ7*
81	NC	D29/PA5	D13*
82	P5.6/~PCE2	DTOUT1/PTD2/~URTS1-0	COM2_RTS/GPIO
83	~WR	R/~W~/PE4	~WR
84	NC	D30/PA6	D14*
85	~RD	NC	~RD/TIP
86	NC	D31/PA7	D15*
87	P5.2	~IRQ6~/PNQ6	GPIO2/IRQ6*
88	ETH_LED0	ETH_LED0	LED_TX/CFG_0
89	ETH_LED1	ETH_LED1	LED_LINK/CFG_1
90	ETH_LED2	ETH_LED2	LED_RX/CFG_2
91	TPOP	Ethernet Tx+	Ethernet_Tx+
92	TPIP	Ethernet Rx+	Ethernet_Rx+
93	TPON	Ethernet Tx-	Ethernet_Tx-
94	TPIN	Ethernet Rx-	Ethernet_Rx-
95	P5.1/CAN_RX	CANRX/PAS3/URXD2	CANRX
96	P5.0/CAN_TX	CANTX/PAS2/UTXD2	CANTX
97	A18	A18/PF2	A18
98	P4.3/~CE3	~CS2~/PJ2	GP_CS2
99	NC	VRH	5P0V_REF*
100	nCE1	~CS1~/PJ1	GP_CS1
101	NC	VDDA/VDDH	5P6V_VCC*
102	P6.7/TXD2	UTXD0/PUA0	COM3_TXD
103	P6.6/RXD2	URXD0/PUA1	COM3_RXD_
104	A21	A21/PF5/~CS4	A21
105	P6.3/~CE7	SIZ1/PE3/SYNCA	~LDAC/~GPIO
106	P6.2/~CE6	DTIN1/PTD3/~URTS1-0	COM3_DTR/GPIO
107	P6.1/~CE5	DTIN0/PTD1/~UCTS1-0	COM3_DSR/GPIO
108	P6.0/~CE4	~CS3~/PJ3	GP_CS3
109	A5	A5/PH5	A5
110	NC	QSPI_CS2/PQS5	SPI_CS2*
111	A6	A6/PH6	A6
112	NC	NC	NC
113	A7	A7/PH7	A7
114	8MHz	8MHz	8MHz
115	200KHz	200KHz	200KHz

116	LOCAL1W	SIZ0/PE2/SYNCB	LOCAL1W/GPIO
117	14.3MHz	14.3MHz	14.3MHz
118	VPULLUP	VPULLUP	VPULLUP
119	VCC_BAT	VSTBY	VSTBY
120	SCK_1	QSPI_CLK/PQS2	SPI__SCK
121	MO_1	QSPI_DOUT/PQS0	SPI_MO
122	MI_1	QSPI_DIN/PQS1	SPI_MI
123	SPI_CS0	QSPI_CS0/PQS3	SPI_CS0
124	SPI_CS1	QSPI_CS1/PQS4	SPI_CS1
125	PLD_GEN0/PLD_X0	GPTA0/PTA0	GPIO4
126	PLD_GEN1/PLD_X1	GPTA1/PTA1	GPIO5
127	PLD_GEN2/PLD_X2	GPTA2/PTA2	GPIO6
128	PLD_GEN3/PLD_X3	GPTA3/PTA3	GPIO7
129	PLD_GEN4/PLD_X4	AN0/PQB0/ANW	GPIO8
130	PLD_GEN5/PLD_Y0	AN1/PQB1/ANX	GPIO9
131	PLD_GEN6/PLD_Y1	AN2/PQB2/ANY	GPIO10
132	PLD_GEN7/PLD_Y2	AN3/PQB3/ANZ	GPIO11
133	PLD_GEN8/PLD_Y3	AN52/PQA0/MA0	GPIO12
134	PLD_GEN9/PLD_Y4	AN53/PQA1/MA1	GPIO13
135	NC	AN55/PQA3/ETRIG1	GPIO14
136	NC	AN56/PQA4/ETRIG2	GPIO15
137	JTAG_TDI	GPTB1/PTB1	JTAG_TDI
138	JTAG_TDO	GPTB2/PTB2	JTAG_TDO
139	JTAG_TCK	GPTB0/PTB0	JTAG_TCK
140	JTAG_TMS	GPTB3/PTB3	JTAG_TMS
141	3.3VCC	3.3VCC	3.3VCC
142	3.3VCC	3.3VCC	3.3VCC
143	GND	GND	GND
144	GND	GND	GND

