

USING THE REMOTE ACCESS DEVICE

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DISCLAIMER

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FCC COMPLIANCE

The RAD is classified as a sub-assembly per FCC CST bulletin, #62, May 1984. The bulletin states that sub-assemblies are not themselves subject to the FCC rules. Only the end product is directly subject to the rules.

HARDWARE DESCRIPTION

The Remote Access Device (RAD) may be powered by a 8 to 15 volt DC supply by connecting to JK1 and installing a jumper in JP6. The power supply jack sleeve should be ground and the center +V. Also, the RAD may instead be powered by a 5V supply if JP 6 is removed and screw terminal 1 is installed.

A RAD without the I/O upgrade will only have ST1 pins 1 and 2. The pinout for ST1 on a board with the I/O upgrade (consisting of 2 relays and an optically coupled input) is as follows:

ST1 pinout

- 1 Vcc This can be a +5V input if JP6 is removed or an output if JP6 is in.
- 2 GND Ground
- 3 INA INA and INB are the two connections for the optically coupled input.
- 4 INB 5, 24 or 120 volts AC or DC may be directly applied here if JP2 is properly configured. See chart below:
 - 5V JP2 position A
 - 24V JP2 position B
 - 120V JP2 empty. SEE WARNING BELOW
- 5 K1A K1A and K1B are the 2 switch connections for the normally
- 6 K1B open relay #1.
- 7 K2A K2A and K2B are for relay #2.
- 8 K2B

The relay contacts are rated at 100VDC/130VAC. The contact rating for a resistive load is 10VA. The max switching current is 0.5 amps with a max carry current of 1.5 amps. If high voltage/current loads are being switched using the relays, a MOV or snubber should be placed in parallel with the relay switches.

WARNING

Caution should be used when applying 120V to pins 3 and 4 or to the relay pins 5,6,7 and 8. The RAD must be properly enclosed and electrically insulated to prevent accidental touching or shorting of the circuit board, since some tracks, pins, and screw terminals can carry a lethal voltage. The enclosure should never be opened while high voltage is being applied to the RAD.

SERIAL PORTS

HDR1 (COM1) is the main communication port. If it is connected to a PC serial port, the RAD can be held in reset by asserting the DTR line. Since most PC based terminal emulators do this by default, the RAD will not be able to communicate with a terminal emulator unless the DTR line is de-asserted or unless HDR1 pin 7 is left disconnected. The HDR1 pinout is as follows:

HDR1 RS-232			HDR1 RS-422/485		
1	2		1	2	
nc	.	nc	nc	.	nc
Tx	.	nc	TxB	.	RxA
Rx	.	nc	TxA	.	RxB
DTR	.	nc	DTR	.	nc
GND	.	nc	GND	.	nc
9	10		9	10	

If the RS-422/485 option is installed, JBLK1 will also be installed and a jumpers when installed in positions 1 through 6 will perform the following:

JBLK1

- 1 . . This connects TxA to RxA.
- 2 . . This connects TxB to RxB.
- 3 . . This pulls RxA up to Vcc through a 36K resistor.
- 4 . . This pulls RxB to ground through a 36K resistor.
- 5 . . This places a 120 ohm terminating resistor across RxA and RxB.
- 6 . . This places a 120 ohm terminating resistor across TxA and TxB.

If the unit is ordered with the optional second serial port, HDR2 (COM2) is installed and is defined as follows:

	HDR2	
	RS-232	
	1	2
nc	. .	nc
Tx	. .	nc
Rx	. .	nc
nc	. .	nc
GND	. .	nc
	9	10

LCD CONNECTORS

Connectors LCD1 and 2 are for character LCD or VFD displays and also provides backlighting capability by configuring jumpers JP3,4. For connectors without pin 1 indicated, look on the opposite side of the connector where it is soldered on the board and you will notice that one of the four corner pads is more square than the others; this is pin 1. LCD2 is pin for pin the same as LCD1 except it is 16 pins in a single row connector instead of double row. Pin 1 of the LCD2 connector is the pin closest to LCD1.

On power-up there is a delay before initializing the display to allow it time to power-up. This is necessary for systems that have vacuum fluorescent displays.

	LCD1			LCD2											
	1	2		1											16
GND	. .	Vcc												
CONTRAST	. .	LCD RS													
LCD R/W	. .	LCD E													
nc	. .	nc													
nc	. .	nc													
LCD D4	. .	LCD D5													
LCD D6	. .	LCD D7													
(JP3)	. .	(JP4)		JP3 and JP4 must be in position B for backlight											
	15	16													

KEYPAD CONNECTOR

This connector allows interfacing to a 4x4 keypad. If the second serial port is not installed, Y5 is available so a 4x5 keypad can be scanned.

HDR3	1								9	SP1
	Y5
	X4	X3	X2	X1	Y4	Y3	Y2	Y1	GND	

MISCELLANEOUS CONNECTORS

This connector gives direct access to all the port lines of the microcontroller plus Vcc, ground and the active high reset input.

```

HDR4
 1   2
RX1 . . Beeper circuit driver
TX1 . . RS 485 TX ENABLE
LED1 . . KEYPAD Y5 (or RX2 for 2nd serial port)
LED2 . . LED4A (or TX2 for 2nd serial port)
LED3 . . LED4D (LED4 when 2nd serial port installed)
OPTO IN . . rsv
RELAY1 . . rsv
RELAY2 . . rsv
RESET . . nc
LCD RS . . KEYPAD Y1
LCD R/W . . KEYPAD Y2
LCD E . . KEYPAD Y3
LCD E2 . . KEYPAD Y4
LCD D4 . . KEYPAD X1
LCD D5 . . KEYPAD X2
LCD D6 . . KEYPAD X3
LCD D7 . . KEYPAD X4
nc . . nc
nc . . GND
39   40

```

Note that since these pins are directly connected to the microcontroller they are 0 to 5V signals and there may be driving or conditioning circuitry already connected to the line as well. For example, if all options are installed the RX1, RX2, and OPTO IN pins on this header will be driven by external circuitry, so you should not attempt to drive them through this connector. The OPTO IN, RELAY1 and RELAY2 pins can be used here when the I/O option is not installed. Remember that the OPTO IN pin can only accept 0-5V levels and note that the RELAY1 and 2 pins are active-low.

HDR5 gives alternative access to the speaker output and the active low output ports that control the LEDs.

```

HDR5
 1   2
Vcc . . Vcc
GND . . GND
LED1 . . LED2
LED3 . . LED4
BEEP+ . . BEEP-
 9   10

```

HDR6 is a good connector to access Vcc, ground and the active high reset input. If a jumper is installed across pins 9 and 10 when the RAD comes out of reset, this will start configuration mode (discussed later). The pins marked "rsv" are reserved and should be left unconnected.

```

HDR6
 1   2
RST . . Vcc
rsv . . nc
rsv . . nc
rsv . . nc
CFG . . GND
 9   10

```

INSTANT MODE PROTOCOL

The RAD is shipped from EMAC configured in instant mode. To change modes, see POLLED MODE PROTOCOL. In instant mode, all characters sent to the RAD with an ASCII code less than 80h and greater than 9fh will interpreted as display data or single byte control characters.

Following is a list of standard ASCII control characters that are used by the RAD:

07H Bell:	Turn on the beeper momentarily
08H Backspace:	Move cursor 1 space back
0AH Linefeed:	Move cursor to other line
0DH Carriage return:	Move cursor to beginning of current line
1AH Clear Screen:	Clear display and move cursor to home
1EH Home:	Move cursor to upper left corner

This should allow simplified code since many languages support carriage return and linefeed as an inherent part of their output functions.

COMMANDS

The following are the commands supported by the RAD in instant mode:

- 80H Resync command. Sending 80H by itself will return the RAD to a known state. It is a good practice to do this as the first step of initialization. To understand the purpose of this command, consider the following: If the state of a particular RAD was not known, it could possibly be waiting for the second byte of a 2 byte command. When the 80H is received, it will be used as the data in this case. If the RAD was not waiting for a 2nd byte the 80H is simply ignored.
- 82H Return the firmware version for the RAD as 0FEH followed by two bytes of the version #.
- 84H Return Unit Status command. The response to this command is described in the RETURN CODES section.
- 86H Initialize the display type specified by the byte that follows. Currently the only type supported is 0 which is for standard character displays.
- 88H Send the byte following this command to the display command register.
- 8AH Repeat the last character sent to the display the number of times selected by the byte following this command.
- 8CH Write to control register command. The control register can be manipulated 2 ways. The easiest way is to follow the register command with one of the following bytes:
 - 01H Turn relay 1 off (default)
 - 02H Turn relay 1 on
 - 03H Turn relay 2 off (default)
 - 04H Turn relay 2 on
 - 05H Send no response when opto-input changes state
 - 06H Send response when opto-input changes state (default).
 - 07H Select single character response to opto-input change of state. Send "Q" (51H) on a falling edge, and "R" (52H) on a rising edge (default).
 - 08H Select a dual character response. The header 0FDh, will be sent followed by the unit status (the same response as received from a Return Unit Status command).

The second method is used when it is desired to have direct control over the register. When bit 7 of the second byte is set, the rest of the byte is written to the control register. For example, if the value of the second byte has bit 7 set then:

- Bit 0 would control relay 1 (1=on, 0=off)
- Bit 1 would control relay 2 (1=on, 0=off)
- Bit 2 if set, would cause a response to be sent when the opto-input changes state.
- Bit 3 would define the type of response sent. If 0, a "Q" (51H) will be sent on a falling edge, and "R" (52H) will be sent on a rising edge. If 1, the header 0FDh, will be sent followed by the unit status (the same response as received from a Return Unit Status command).

- 8EH Turn on LEDs according to the pattern in the data byte following the command. Setting any of bits 0 - 3 in this data byte will turn on LEDs 1 - 4, respectively.
- 90H Write packet to COM2 transmit buffer. The byte following this command is the length byte which indicates the number of data bytes to follow the length byte. If the packet is not completed within the timeout period, the command is aborted after sending the characters received up to that point.

RETURN CODES

The following codes are returned from the RAD in instant mode:

- 0FCH,x This is the header character for the packet that was received in the COM2 buffer. The byte following this is the length byte which indicates the number of data bytes to follow the length byte. A packet is defined as one or more characters received followed by a delay.
- 0FDH,x This is sent in response to the Return Unit Status command (or, if programmed to do so, in response to a transition on the opto-input), where x is the status byte which is formatted as follows:

BIT	DESCRIPTION
0	Relay 1 state: 0=off, 1=on
1	Relay 2 state: 0=off, 1=on
2	Opto-input state: 0=off, 1=on
3	Set when COM2 transmitter is busy sending a packet.
4-7	(reserved)
- 0FEH,x This is sent in response to the Return Firmware Version command, where x is the version number.
- 0FFH,01H This is sent when an invalid character or command was received.
- 0FFH,02H This is sent if the RAD receive buffer overflows.

The intersection of any one of HDR 3 pins 1-4 with any one of pins 5-8 will cause an ASCII character to be sent out of the RAD serial port. The charts below show the character returned at each intersection:

KEYPAD DECODING CHART

	4	3	2	1
8-	A	B	C	D
7-	E	F	G	H
6-	I	J	K	L
5-	M	N	O	P

SP1- Q R S T (SP1 is only available on RADs without a 2nd UART)

ASCII CHART

ASCII CODE	ASCII CHARACTER	ASCII CODE	ASCII CHARACTER
41H	A	49H	I
42H	B	4AH	J
43H	C	4BH	K
44H	D	4CH	L
45H	E	4DH	M
46H	F	4EH	N
47H	G	4FH	O
48H	H	50H	P

POLLED MODE PROTOCOL

A RAD is normally shipped configured in instant mode, but it may be configured to polled mode by using the configuration utility included on the distribution disk.

COMMAND PACKET STRUCTURE

When configured in polled mode, with one master (typically a PC) you may communicate to one or more slave RADs through the following basic packet structure:

<addr>,<len>,<pckt#>,<cmd>,[x,...],<crchi>,<crclo>

<addr> This is the slave address byte which determines the destination for the packet. If <addr> is 0, this is the broadcast address, meaning the data is for all RADs in the network. Otherwise it is for only the RAD that has the matching address in the range from 1 to 254 (255 is reserved for future revisions). The RAD detects the start of a packet in one of two ways based on the mode. In 9 bit mode the <addr> must be sent with the 9th bit set and all other bytes in the packet must have the 9th bit clear. In 8 bit mode the RAD receiver must have 50mS of inactivity before receiving <addr>, otherwise the whole packet will be ignored.

<len> This indicates the number of bytes to follow, excluding the CRC bytes. Packets must be less than 60 characters or they will be ignored, so *a packet should always have a <len> of less than 56.*

<pckt#> This is the packet number and it can be used by the RAD to detect if a command is being repeated if this feature is enabled when the RAD is configured. In the case where the master doesn't get a good response from a RAD, (whether caused by the RAD detecting a data error in its received packet and not responding, or by the MASTER detecting a data error in the packet that came back from the RAD) the master should resend the same packet with the same packet number. When the RAD sees a new packet number it will respond to the packet as is normal, but if the packet number is the same as the previous one received it will re-send the same response it sent the last time it received the packet number. When the packet number detection feature is enabled, it is very important that the number change if different packet information is being sent, because if two packets are sent each using the same packet number the response to the second packet will be the same as the response sent for the first one even if the second packet had a different command. The use of packet numbers is necessary because if a read buffer command was executed and the master, for whatever reason, didn't get the data and the RAD were to merely execute the command again, the data read would only be the characters that were buffered from the time of the first command to the second. Also if an output command were executed and the master was expecting an acknowledgment but the packet returned by the RAD was corrupted, the master will resend the packet but this time the RAD will not perform the action but only return the acknowledgement again.

<cmd> This is the command (the definitions are listed below).

[x,...] This is the write data field of 0 (empty) or more bytes of data specific to the command being sent. Most commands have individual limits on the size of this field.

<crchi>,<crclo> These bytes make up the 16 bit error checking word. The word is generated from a seed of FFFF hex and is modified by each byte in the packet (including <addr> and <len>, but excluding the 2 CRC bytes themselves). If the RAD is configured to perform CRC checking, only packets without CRC errors will be processed. If CRC checking is disabled, dummy bytes of any value should be sent in place of them, but they will be ignored.

RESPONSE PACKET STRUCTURE

All commands that are successfully processed, except Reset (80h), can return a response packet. However, returning a response packet is not desirable when there are multiple slave RADs and a broadcast packet is sent (<addr> = 0), since they will all try to respond at the same time. For this reason there is a configuration option which can disable responses to broadcast packets on all commands except Return Firmware Version. This command always returns a response, so it should not be broadcasted in a multi-slave network.

Since multiple RADs may be connected to the master, a slave RAD does not send a response to a packet that has a CRC error. This is necessary because the address may have been corrupted and since the packet may have been intended for another meter anyway, sending data would only contend with the returned data of the intended recipient.

The response packet has a structure similar to the command packet.

<addr>,<len>,<pckt#>,<ack>,<stat1>,<stat2>,[x,...],<crchi>,<crclo>

<addr> This is the address of the RAD sending the response packet.

<len> This is the number of bytes to follow, excluding the CRC bytes.

<pckt#> This is the same packet number that was sent to the RAD.

<ack> This is the command acknowledge which is 1 + the command number received.

<stat1> This is the first byte of status bits.

Bit	Definitions
0	Configuration data error
1	unit has been reset
2	bad command received
3	bad packet received
4-7	(reserved)

<stat2> This is the second byte of status bits.

Bit	Definitions
0	keypad buffer overflow
1	COM1 Rx queue overflow
2	COM2 Rx queue overflow
3	COM2 Rx queue has received a packet.
4	keypad has data
5	COM2 Tx buffer is below level specified by <c2txlo> (see CONFIGURATION MODE).
6	opto-in has changed state
7	COM2 Rx buffer is above level specified by <c2rxhi> (see CONFIGURATION MODE).

[x,...] This is the return data field containing 0 to 248 bytes returned by the RAD. There are many different structures for this field depending on the command, and on some this field is empty.

<crchi>,<crclo> These bytes make up the 16 bit error checking word. The word is generated from a seed of FFFF hex and is modified by each byte in the packet, (including <addr> and <len>, but excluding the 2 CRC bytes themselves).

POLLED MODE COMMANDS

Following is the list of commands and the unique structures for the write data fields and the resulting return data fields.

- All commands are even numbered and greater than or equal to 80h.
- All commands return a response packet (except in the cases discussed previously).
- Commands must be sent in the format of the command packet structure, and response packets are returned in the format of the response packet structure.

80H Reset.

This does a software reset of the RAD, which also applies the configuration parameters that were last written with the Write Configuration command. This command never returns a response, however, after the RAD has been reset, polling the status flags will indicate that the unit has been reset.

Write data field structure: (empty data field)

82H Return the firmware version and status for the RAD.

This command always returns a response, so care must be taken to avoid sending it with a broadcast address in a multi-slave network.

Write data field structure: (empty data field)

Return data field structure: <cpu>,<ver>

Where: <cpu> is the CPU type 0=standard Atmel, 1=standard Dallas.

<ver> is the firmware version number.

84H Return RAD status.

Write data field structure: (empty data field)

Return data field structure: (empty data field)

86H Initialize the display.

Write data field structure: (empty data field)

Return data field structure: (empty data field)

88H Write to display command register

Send the byte following this command to the display command register.

Write data field structure: <dcmd>

Where: <dcmd> is the byte sent to the display's command register.

Return data field structure: (empty data field)

8AH Character repeat

Repeat the last character sent to the display the number of times selected by the byte following this command.

Write data field structure: <rept>

Where: <rept> is the number of times the character is to be repeated.

Return data field structure: (empty data field)

8CH Position and display characters

Position the display cursor at the selected x,y coordinates and then show any optional bytes that may follow as text on the display. If you leave off the optional display characters, this command can be used for cursor positioning.

Write data field structure: <xcor>,<ycor>, [<dsp1>...<dsp30>]

Where: <xcor>,<ycor> are the x and y coordinates to position the cursor.

[<dsp1>...<dsp30>] are 0 to 55 optional characters to show on the display.

Return data field structure: (empty data field)

8EH Display characters

Display the bytes that follow the command at the current cursor position.

Write data field structure: [*<dsp1>...<dsp30>*]

Where: [*<dsp1>...<dsp30>*] are 0 to 55 characters to show on the display.

Return data field structure: (empty data field)

90H Write the byte following this command to the control register

The control register can be manipulated 2 ways. The easiest way is to follow the register command with one of the following bytes:

01H Turn relay 1 off (default)

02H Turn relay 1 on

03H Turn relay 2 off (default)

04H Turn relay 2 on

The second method is used when it is desired to have direct control over the register. When bit 7 of the second byte is set, the rest of the byte is written to the control register. For example, if the value of the second byte has bit 7 set then:

Bit 0 would control relay 1 (1=on, 0=off)

Bit 1 would control relay 2 (1=on, 0=off)

Write data field structure: *<cntl>*

Where: *<cntl>* is the byte written to the control register

Return data field structure: (empty data field)

92H LED output

Turn on LEDs according to the pattern in the data byte following the command. Setting any of bits 0 - 3 in this data byte will turn on LEDs 1 - 4, respectively.

Write data field structure: *<LED>*

Where: *<LED>* is the byte written to the LEDs.

Return data field structure: (empty data field)

94H Write the bytes following this command to the COM2 transmit buffer

Write data field structure: [*<char1>...<char30>*]

Where: [*<char1>...<char30>*] represents 0 to 30 characters to be written to the COM2 transmit buffer.

Return data field structure: (empty data field)

96H Read data from the COM2 receive buffer

If there is no data, the length byte will be 4 which is the length of a packet with an empty data field.

Write data field structure: (empty data field)

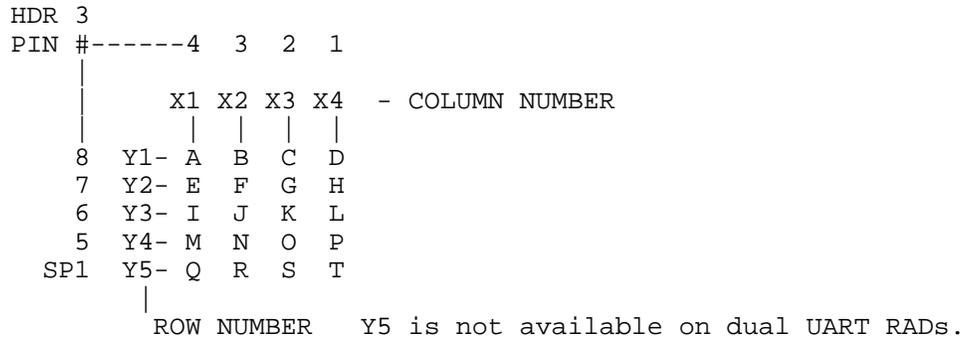
Return data field structure: [*<char1>...<char30>*]

Where: [*<char1>...<char30>*] represents 0 to 30 characters that have been read from the COM2 receive buffer.

98H Read data from the keypad buffer

If there is no data, the length byte will be 2 which is the length of a packet with only the command ack and packet number returned.

The RAD keypad scanner looks for a connection between the row and column pins. The characters shown below at the intersection of the X and Y coordinates are buffered when such a connection is made. Keypad scan codes:



Write data field structure: (empty data field)
Return data field structure: [*<key1>*....*<key8>*]
Where: [*<key1>*....*<key8>*] represents 0 to 8 keys that have been read from the buffer.

9AH Read data from the opto-isolated input status register

Bit 0 of the byte returned contains the present status of the input. Also, subtracting the previous value read from the present value will indicate how many transitions have occurred since the previous reading.

Write data field structure: (empty data field)
Return data field structure: *<opto>*
Where: *<opto>* is the opto-isolated input status register.

9CH Write to the configuration registers

The values written will not become active until the RAD is reset, or until the Reset command is executed. See CONFIGURATION MODE section for a more detailed description of the registers. Note that the RAD doesn't necessarily need to be in configuration mode to use this command.

Write data field structure:
<cfg1>,*<cfg2>*,*<addr>*,*<dlay>*,*<rxto>*,*<dsptype>*,*<c2rxhi>*,*<c2txlo>*,*<2 reserved bytes>*
Return data field structure: (empty data field)

9EH Read the configuration registers

See CONFIGURATION MODE section for a more detailed description of the registers.
Write data field structure: (empty data field)
Return data field structure:
<cfg1>,*<cfg2>*,*<addr>*,*<dlay>*,*<rxto>*,*<dsptype>*,*<c2rxhi>*,*<c2txlo>*,*<2 reserved bytes>*

A0H Read data last written to the control register

Write data field structure: (empty data field)
Return data field structure: *<ctrl>*
Where: *<ctrl>* is the data last written to the control register (see write control register command).

- Bit definition of *<ctrl>*
- Bit 0 indicates status of relay 1 (1=on, 0=off)
 - Bit 1 indicates status of relay 2 (1=on, 0=off)
 - Bit 2 indicates status of opto-input (1=on, 0=off)

CONFIGURATION MODE

If a Jumper is installed across pins 9 and 10 of HDR6 during reset or power-up starts CFG mode at 9600-8-N-1. If a terminal emulator such as Hyperterminal^(C) is running on your PC and is connected to the RAD, the message "CFG MODE" will be displayed on the PC. Characters typed at the PC will be echoed back and displayed on the PC as long as the jumper is still installed. If for some reason the RAD needs to be reconfigured into instant mode, pressing ESC on your PC will cause the message "INST MODE" to be displayed. Removing the jumper from HDR6 will cause the configuration to be stored. If HDR6 is not removed and the RAD is reset, it will retain the original configuration.

When the HDR6 jumper is removed and ESC has not been pressed, group 1 configuration flags will be set to 00000001b, without storing them to NV memory. These flag settings will do the following: enable 8 bit mode, enable responses from broadcast packets, and packet numbers and CRC's will be ignored.

In configuration mode, the broadcast address (0) should be used to configure the RAD since the unit's address may not be programmed yet. In CFG mode the RAD returns data even when a broadcast packet is sent, therefore in this mode only 1 slave should be connected to the master.

The read data field and write data field structures are defined as:

<cfg1>,<cfg2>,<addr>,<dlay>,<rxto>,<dsptype>,<c2rxhi>,<c2txlo>,<2 reserved bytes>

Where:

<cfg1> Group 1 of configuration flags

Bit	Definition
0	Set if polled mode, clear if instant mode.
1	Set if 9 bit, clear if 8 bit.
2	Set to disable response to broadcast packets.
3	Clear to ignore packet numbers.
4	Clear to ignore CRC bytes.
5	Set to enable beep on key press.
6	(undefined)
7	(undefined)

<cfg2> Group 2 of configuration flags

Bit	Definition
0	(undefined)
1	(undefined)
2	(undefined)
3	(undefined)
4	(undefined)
5	(undefined)
6	(undefined)
7	(undefined)

<addr> This allows defining of a unique RAD address. The RAD uses this address to determine which packets it is supposed to process.

<dlay> This byte defines the amount of delay desired before sending a response. This is necessary in situations where there is 2 wire multi-drop and the master may not have instant control of its RS485

transmitter enable line. This allows the RAD to wait a predetermined amount of time to allow the master's transmitter to disable before sending a response. Otherwise, if the RAD responded while the master transmitter was still enabled, the transmitted data would be corrupted due to contention on the twisted pair. The minimum delay is based on the delay value times 25mS. In addition, a delay value of 0 gives a delay of 5mS.

<rxto> This defines the amount of time the receiver must be inactive before the receive buffer will reset itself. In 8 bit mode this defines how long there must be inactivity on the network before a new packet can be received. In 9 bit mode the delay does not determine the start of a packet. In both 8 and 9 bit mode a packet will be discarded if the time between any 2 characters is larger than this timeout value. The minimum delay is based on the delay value times 25mS. A value of 2 or greater should be used.

<dsptype> This defines the type of display connected to the RAD. The following types are defined:

- 1: 20x2 Character display
- 2: 20x4 Character display

<c2rxhi> This is the COM2 Rx queue high level setpoint. When the queue fills past this level, a flag is set in *<stat2>*. When the queue is emptied below this level with the Read COM2 queue command, the flag will be cleared.

<c2txlo> This is the COM2 Tx queue low level setpoint. When the queue empties below this level, a flag is set in *<stat2>*. When the queue is filled above this level with the Write to COM2 queue command, the flag will be cleared.

<2 reserved bytes> These are reserved for future revisions.